EES2
ENERGY
EFFICIENCY
SCALING

PLEDGE SIGNING CEREMONY

June 24, 2025

ABOUT EES2

The Energy Efficiency Scaling for Two Decades (EES2) initiative is our proactive response to the rapidly increasing energy needs for microelectronics applications, especially compute (SRC 2022). Current forecasts reveal that energy use could potentially triple by 2028 in high-growth scenarios, making energy efficiency an essential component of any plan to reliably meet the energy needs of our compute demand for years to come (LBNL 2024).

Our initiative targets energy usage across the microelectronics sector—from burgeoning datacenters to the anticipated demands of 6G communications, with the former serving the advancement of high-performance computing, AI, and quantum computing. With a strategic plan crafted by DOE's Advanced Materials & Manufacturing Technologies Office (AMMTO), EES2 is ambitiously set to counter the rising energy demand by doubling microelectronics energy efficiency every two years.

This initiative is not just about innovation; it's about swift action and broad collaboration. With the roadmap effort having started in 2022, our immediate next steps after publishing the roadmap in 2025 are to gather public input and deploy commercially ready technologies by the end of 2025.

Our goal extends beyond technological advancement; it encompasses building a skilled workforce capable of both developing and manufacturing these critical technologies. As we gather here today, we stand united with over 70 organizations that have pledged, alongside DOE, to champion this cause, ensuring that we stay on an aggressive path toward energy efficiency in microelectronics.

THE EES2 PLEDGE

We the undersigned agree to cooperate

- To document and learn from the extraordinary record of microelectronics', including power electronics', energy efficiency such as increases greater than 1,000,000x in energy efficiency since the invention of the transistor nearly 75 years ago;
- To document and learn from microelectronics' past and forecasted future ability to enable all sectors of the economy to benefit from rapid innovation in computing and communication through extreme energy efficiency;
- To identify and publicize problems solved and opportunities offered by microelectronics' Energy Efficiency Scaling over 2 Decades (EES2);
- To participate in the AMMTO-led EES2 2025-2026 R&D roadmapping effort;
- To coordinate promising EES2-inspired R&D projects among partners; and
- To explore formation of a partnership, an "EES2 Alliance" that enables the EES2 1000X efficiency increase goal by leading EES2 R&D roadmapping after 2025 and by catalyzing the deployment of cost-effective technologies, including power electronics, needed to stay on the EES2 path of doubling microelectronics' energy efficiency every two years.

We do this because

- Microelectronics' life-cycle energy use is accelerating so rapidly that extreme energy efficiency is necessary to maintain competitive innovation in the near-, mid-, and long-term.
- EES2's extreme energy efficiency increases are necessary to do more, faster in critical microelectronics applications such as computing—including AI—and communication.
- EES2 is a key organizing principle that enables us to meet new energy demands affordably and reliably.
- EES2 is a technology leadership path that provides economic, national security, and other public benefits.

Shannon Bragg-Sitton

Associate Laboratory Director

Idaho National Laboratory

Dr. Bragg-Sitton oversees a team of over 350 staff dedicated to a resilient, affordable, and diverse energy agenda. She steers INL's research efforts to deliver viable energy solutions, focusing on microgrid systems, water treatment, critical minerals and materials, advanced manufacturing, and efficient chemical production while harnessing cutting-edge technologies to efficiently integrate nuclear and other energy resources into the grid and the industrial sector.

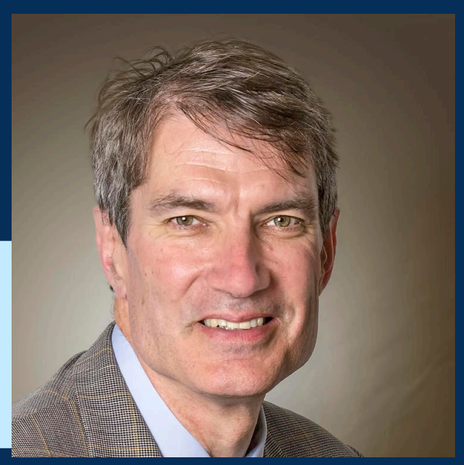
Shannon has earned a bachelor of science in nuclear engineering, master of science in medical physics, and a master of science and doctorate in nuclear engineering.

INL fully supports the Department of Energy's Advanced Materials and Manufacturing Technology Office's effort to create an R&D roadmap aimed at achieving a new energy efficiency scaling goal (EES2) to dramatically improve the energy efficiency of microelectronics by 1000 times over the next two decades. The demand for increased computing power will grow exponentially, driven by the expansion of digitization and artificial intelligence, and our nation must meet this challenge. INL is ready to assist DOE and its partners in this effort.

Steve Cowley

Laboratory Director

PPPL PRINCETON PLASMA PHYSICS LABORATORY



Sir Steven Cowley is a theoretical physicist and international authority on fusion energy. He's laboratory director of the U.S. Department of Energy's Princeton Plasma Physics Laboratory, which is managed by Princeton University, where Cowley is also professor of astrophysical sciences. He's also chair of the Board of Trustees for the Faraday Institution.

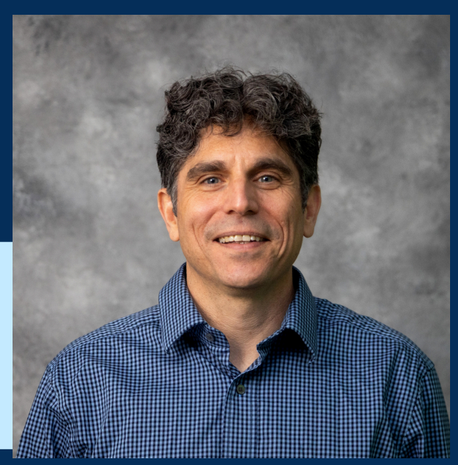
Prior to his current positions, Cowley was president of Corpus Christi College and professor of physics at the University of Oxford in the United Kingdom. Cowley previously was chief executive officer of the United Kingdom Atomic Energy Authority and head of the Culham Centre for Fusion Energy.

Joining this pledge is a demonstration of our commitment to sustainable innovation and aligns with national efforts to reduce the carbon footprint of semiconductor and microelectronics manufacturing. As PPPL expands our research footprint through delivering plasma science and technology expertise to the community, participating in the EES2 initiative connects us within a growing ecosystem of microelectronics institutions and companies. Joining EES2 reflects PPPL's long-term goals in energy efficiency, advanced manufacturing, and applied scientific research as we work with partners to shape expectations and capabilities around sustainable practices for the future of semiconductor R&D.

Christopher Matranga

Carbon Materials Manufacturing Program Lead

NATIONAL ENERGY TECHNOLOGY LABORATORY



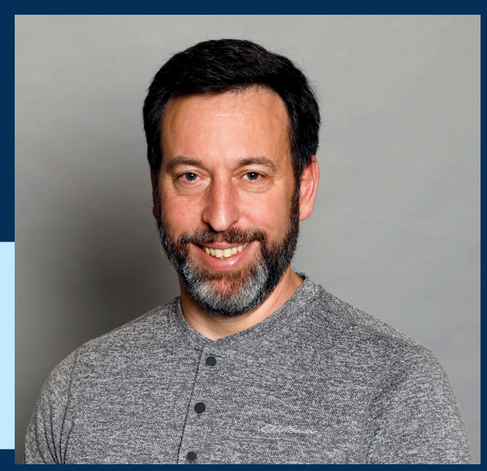
Dr. Christopher Matranga began his career at the National Energy Technology Laboratory (NETL) in 2002 and has held positions as a post-doctoral fellow, research scientist, division director, and senior research fellow. He currently leads NETL's Carbon Materials Manufacturing Program, which focuses on using unconventional feedstocks to manufacture engineered carbon materials for use in microelectronics, batteries, supercapacitors, and structural composites. Dr. Matranga received a Ph.D. & M.S. in chemistry from the University of Chicago, M.B.A. from the University of Pittsburgh, and B.S. in industrial chemistry from the University of Houston-Downtown.

NETL is excited to be part of the EES2 Alliance. This partnership will ensure that the nation's computational capacity, technology development, and economic growth are not limited by the performance and efficiency of the microelectronics we utilize.

Mike Lafferty

CEO

snowcap



Mike is CEO of Snowcap Compute and has a background in digital chip design and fabrication. At Cadence, he led the “More than Moore” customer enablement group, working with companies at the state of the art in quantum, silicon photonics, and superconducting silicon technologies.

Other notable founders of Snowcap Compute:

Anna Herr, Ph.D.: Anna holds a Ph.D. a from Moscow State University and a post-doctorate from Chalmers. Prior to joining Snowcap as chief scientist, she was a Northrup Grumman Fellow focusing on superconducting, as well as science director at imec.

Quentin Herr Ph.D.: Quentin holds a Ph.D. from the University of Rochester and is chief technical officer at Snowcap. Quentin was also a Northrup Grumman Fellow and imec science director and holds numerous patents in superconducting circuit design.

Brian Kelleher: Brian retired in 2024 as senior vice president of Hardware Engineering at NVIDIA, where he oversaw the design and development of industry-leading GPUs, SOCs, and systems. With decades of experience in silicon architecture and product execution, he played a key role in NVIDIA’s growth into AI and high-performance computing.

Phil Carmack: Phil retired in 2024 as vice president of Google’s Platforms and Ecosystems organization, focused on building the silicon foundations for Android and Pixel. Prior to working at Google, he was CEO of Aptina and a senior executive at NVIDIA.

Snowcap’s mission to replace datacenter semiconductors with superconductors to deliver improvements multiple orders of magnitude greater than the current state of the art in energy efficiency aligns closely with the goals of EES2. Snowcap is proud to join the 70+ pledgers working to realize EES2’s goal of 1,000X more energy-efficient computing in the next two decades.

Andrew N. Sloss

Computer Scientist

Andrew N. Sloss is a computer scientist, fellow of the British Computer Society, affiliate assistant professor at the University of Washington, and a long-time researcher with nearly 40 years of experience in the computing and semiconductor industry. He has taught and continues to teach engineering, always driven by a deep interest in unconventional computing technologies. Andrew is particularly focused on emerging paradigms, such as reversible computing and ultra-efficient energy solutions that challenge traditional architectures and hold the potential to redefine computational efficiency. Throughout his career, he has observed and analyzed strategies across various companies and roles, recognizing grit as a common factor for success. His professional journey spans from grassroots innovation to global impact, providing him with unique insights into how long-term strategic thinking delivers the most transformative results, echoing the idea that "big things come from humble beginnings," paraphrasing *Lawrence of Arabia*.

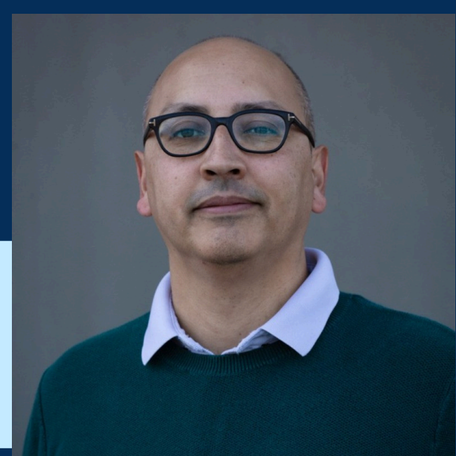
Vaire Computing's core mission aligns directly with the EES2 goal of achieving a 1,000x improvement in semiconductor energy efficiency.

Adiabatic reversible computing is one of the few practical approaches capable of overcoming the thermodynamic limits of conventional CMOS technology. Unlike traditional computing, which dissipates energy as heat with every bit operation, reversible computing can, in principle, perform computations with near-zero energy loss.

James S. Tandon

CEO & Founder

Cassia.ai



James S. Tandon, Ph.D. is the CEO and founder of Cassia.ai, a company that brings advanced arithmetic to bear on the AI power problem. He invented the core custom arithmetic algorithms that Cassia.ai licenses to companies to improve TOPS/watt efficiency. Dr. Tandon earned his doctorate from the University of California Santa Barbara in 2009 before taking a postdoctoral research position at the University of Tokyo in 2009-2013. Before founding Cassia.ai, he worked as an FPGA architect in the Advanced Development Department at Microsemi SoC (now Microchip Technologies) and also as a professor of computer engineering at California State University East Bay.

Cassia.ai was founded for the purpose of solving the AI power problem. With the incredible demands projected to be placed upon our energy resources over the coming decades, we realized early on that we would very soon be hitting a power wall. After developing our custom arithmetic for energy efficiency and compute optimization for AI, we began further exploring new technologies in devices (e.g., superconductors), architecture-level improvements, memory hierarchy, and chiplet optimizations for AI to push the power-performance curve. We found that EES2 aligns perfectly with our vision for an AI future and believe that the strongest advances will come from collaboration with other like-minded organizations. It is an honor for us at Cassia.ai to sign the pledge and join other visionaries in the pursuit of energy efficiency as the best improvements will come from a shared purpose for the future.

Ahmedullah Aziz

Assistant Professor of EECS

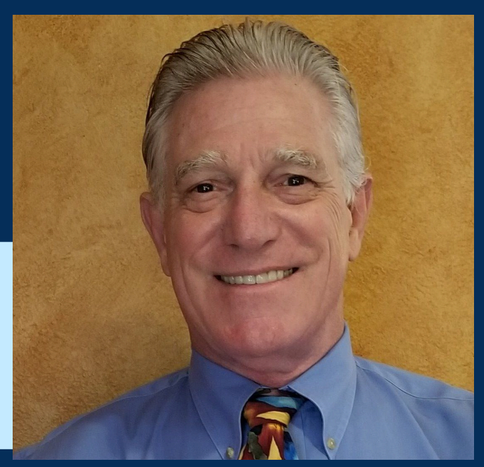
THE UNIVERSITY OF TENNESSEE KNOXVILLE

Dr. Ahmedullah Aziz is an Assistant Professor of EECS at the University of Tennessee, Knoxville, USA. He earned his Ph.D. in ECE from Purdue University in 2019, an M.S. degree in EE from Pennsylvania State University in 2016, and a B.S. degree in EE from Bangladesh University of Engineering & Technology in 2013. He received several awards and accolades for his research, including the Translational Research Award and Chancellor's Innovation Award from UT Knoxville (2024), New Faculty Researcher Award from the American Society of Engineering Educators (2024), ACM SIGDA Outstanding Ph.D. Dissertation Award (2021) from the Association of Computing Machinery, and Outstanding Graduate Student Research Award (2019) from Purdue University. He is a technical program committee member for multiple flagship conferences and a reviewer for several reputed journals (including *Nature* and *Advanced Materials*). He serves as an editorial board member for multiple journals, including *Scientific Reports*, and the *Journal of Applied Physics*. His research portfolio comprises multiple avenues of nanoelectronics, spanning from device modeling to circuit/array design.

At the University of Tennessee, Knoxville, we are committed to advancing the frontiers of energy-efficient electronics through foundational research in superconducting systems and post-CMOS device technologies. Our work focuses on reimagining the core building blocks of computing to overcome the escalating energy demands of AI and data-centric applications. Superconducting electronics, in particular, offer an extraordinary opportunity to break through the energy bottlenecks facing conventional silicon platforms. The EES2 initiative aligns strongly with our mission to enable scalable, low-power, high-performance computing. We are proud to sign this pledge and join a community of researchers and institutions dedicated to building a sustainable and energy-aware technological future.

Bill Gervasi

Principal Memory Solutions Architect



Mr. Gervasi is principal memory solutions architect for Monolithic Power Systems. He has been involved in memory design at the chip, module, and systems level since one kilobit memories were mainstream. He is chairman of the JEDEC Alternative Memories Committee and drives international standards for memory technology in cooperation with all the major data center architects. Mr. Gervasi has been engaged with the EES2 program since its kickoff meeting and has been an active contributor to many sections of the current draft proposal.

Alignment of Monolithic Power Systems and DOE EES2 objectives is clear. MPS is a market leader in high-efficiency power management for a wide range of applications, from handheld devices to data centers. With over 4,000 products and 30,000 customers, MPS is well-positioned to positively impact the goal of reducing the energy consumption of semiconductor applications. MPS pledges to support the EES2 program goal of maximizing the energy efficiency of semiconductors.

Shui-Qing “Fisher” Yu

Distinguished Professor

μ ATOMS

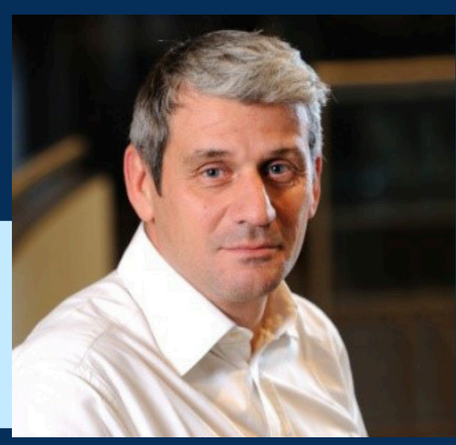
Shui-Qing “Fisher” Yu received his B.S. and M.S. in electronics from Peking University and Ph.D. in electrical engineering from Arizona State University. Dr. Yu currently is a distinguished professor and holds the Twenty-First Century Research Leadership Chair in the Department of Electrical Engineering and Computer Science at the University of Arkansas (UA). His research interests are in developing SiGeSn-based optoelectronic devices (such as lasers and photodetectors) for integrated photonics and infrared imaging applications. He led the Department of Defense Multidisciplinary University Research Initiatives (MURI) center with a focus on using SiGeSn for next-generation mid-IR detector technology and a Department of Energy Energy Frontier Research Center (EFRC) with a focus on the manipulation of atomic ordering for manufacturing semiconductors. He is a fellow of Optica (formerly OSA) and a senior member of IEEE and SPIE.

The “μ-ATOMS” EFRC team is committed to revolutionizing energy-efficient computing, communication, and other microelectronics applications though atomic ordering manipulation of semiconductors.

Nicolas Leterrier

Distinguished Professor

Life Is On | Schneider Electric



Nicolas Leterrier joined Schneider Electric in 2011 and has held several leadership roles in technology and innovation, including vice president of Global Labs. He currently focuses on developing external partnerships within the semiconductor sector.

Nicolas began his career in Paris with Gaz de France and GFInformatique. In 1991, he joined STMicroelectronics as a software development engineer. After working in the U.S. on business development for data storage, he became manager of an application development group in 1999, overseeing projects in telecommunications, automotives, and computer peripherals. He was later appointed software development director for STMicroelectronics' advanced multimedia product line, known as Nomadik architecture, where he led international teams in India and China and established strategic partnerships with major mobile phone manufacturers.

He then joined KIS, a French SME in the photo finishing industry, where he managed the R&D department. From 2006 to 2011, Nicolas served as general manager of Minalogic, a global competitiveness cluster based in Grenoble, France. There, he led initiatives in micro-nano technologies and embedded software, fostering collaboration between industry, academia, and public research institutions. He also initiated several cross-border agreements in the semiconductor field with partners in Germany and the Netherlands.

Nicolas holds a Master of Science degree from Paris XI Orsay University and an engineering diploma from the École des Techniques du Génie Logiciel (School of Software Engineering). He is passionate about resource efficiency in energy, water, and sustainable development. He has led multiple initiatives focused on measuring, understanding, and reducing carbon footprints, as well as integrating renewable energy to minimize environmental impact and resource waste.

Schneider Electric is proud to join the EES2 initiative as a pledging organization, affirming our commitment to advancing energy efficiency and sustainability across the semiconductor value chain. Our support reflects the urgency of addressing the energy intensity of semiconductor manufacturing—especially as demand surges in today's increasingly electrified landscape. Through our Catalyze program and advanced energy management solutions, we are helping suppliers optimize operations through improved energy efficiency and the integration of more distributed and renewable resources. We believe the EES2 roadmap's focus on fostering public-private collaboration, upgrading existing fabs, and improving workforce development is essential to strengthening American competitiveness and achieving national manufacturing leadership goals. Schneider Electric is committed to working alongside DOE and industry partners to turn these goals into action.