EES2 Lightning Talk

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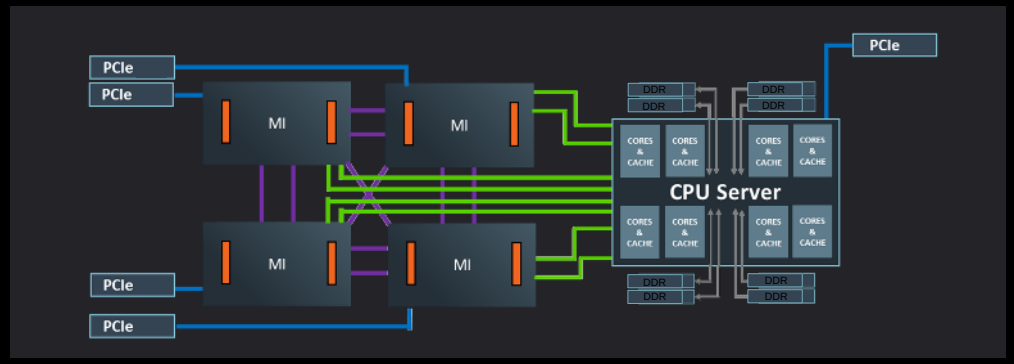
[Public]

AMD's 30x25 Goal

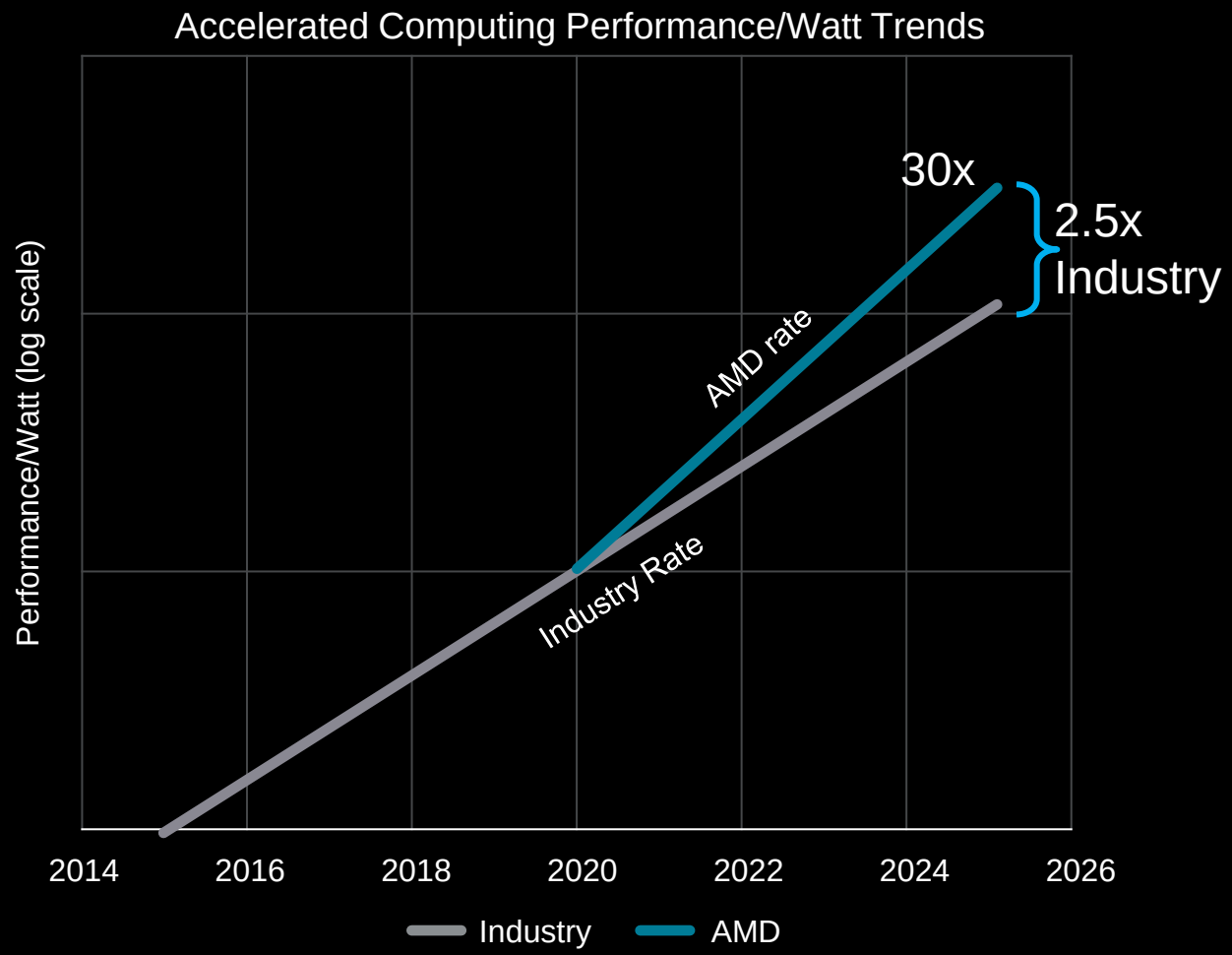
30x increase in energy efficiency for AMD processors and accelerators from 2020-2025*

- Focus on Accelerated Computing nodes using AMD CPUs and GPUs

HPC/ML Node



- Exploit architectural innovations, package and silicon technology advances to change the trend



Based on 2015-2020 industry trends in energy efficiency gains and data center energy consumption in 2025.
* Includes AMD high performance CPU and GPU accelerators used for AI training and High-Performance Computing in a 4-Accelerator, CPU hosted configuration. Goal calculations are based on performance scores as measured by standard performance metrics (HPC: Linpack DGEMM kernel FLOPS with 4k matrix size. AI training: lower precision training-focused floating point math GEMM kernels such as FP16 or BF16 FLOPS operating on 4k matrices) divided by the rated power consumption of a representative accelerated compute node including the CPU host + memory, and 4 GPU accelerators.

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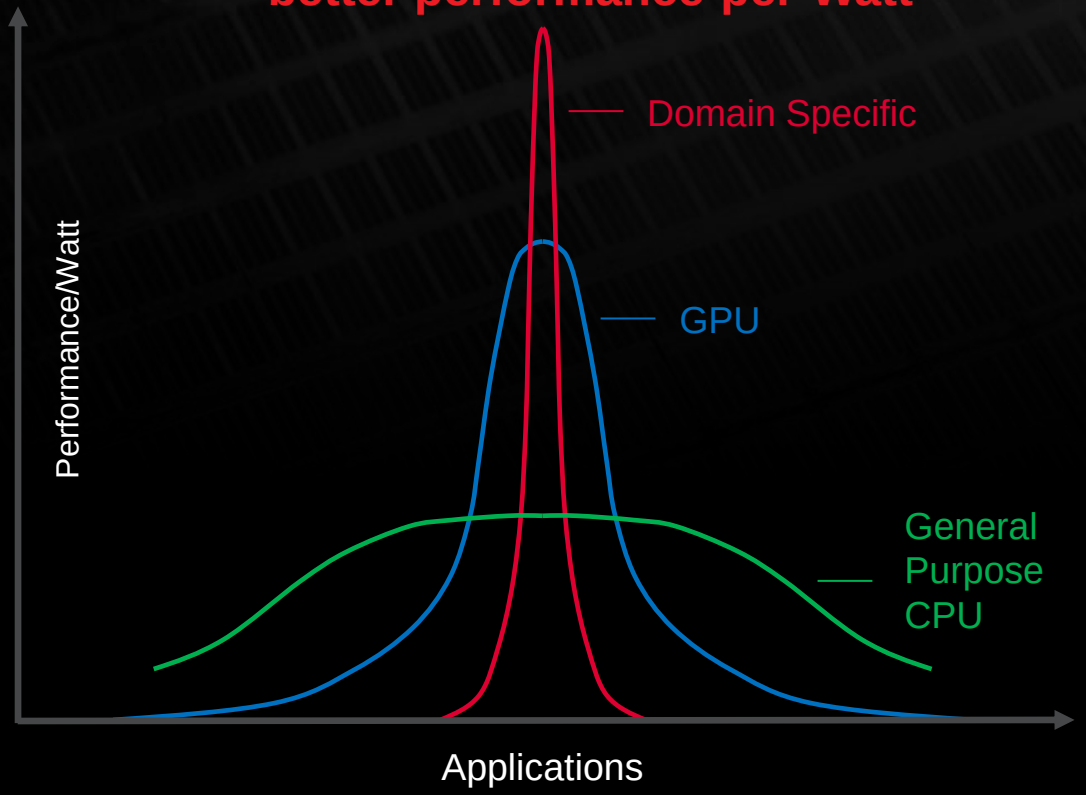
Efficiency through Domain Specific Architectures and Package Innovation

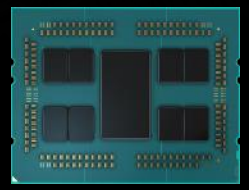
Application-Specific optimization provides better performance-per-Watt



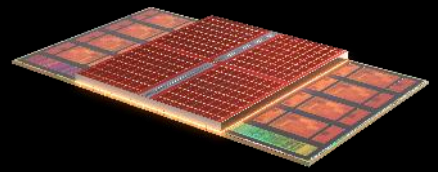
AMD is leading the way in finding new approaches to reduce energy for compute

Modular design, chiplets, and 3D stacking are the next frontier for efficiency gains

CHIPLETS → **3D CHIPLETS**



(Chiplet + Advanced 3D Stacking)



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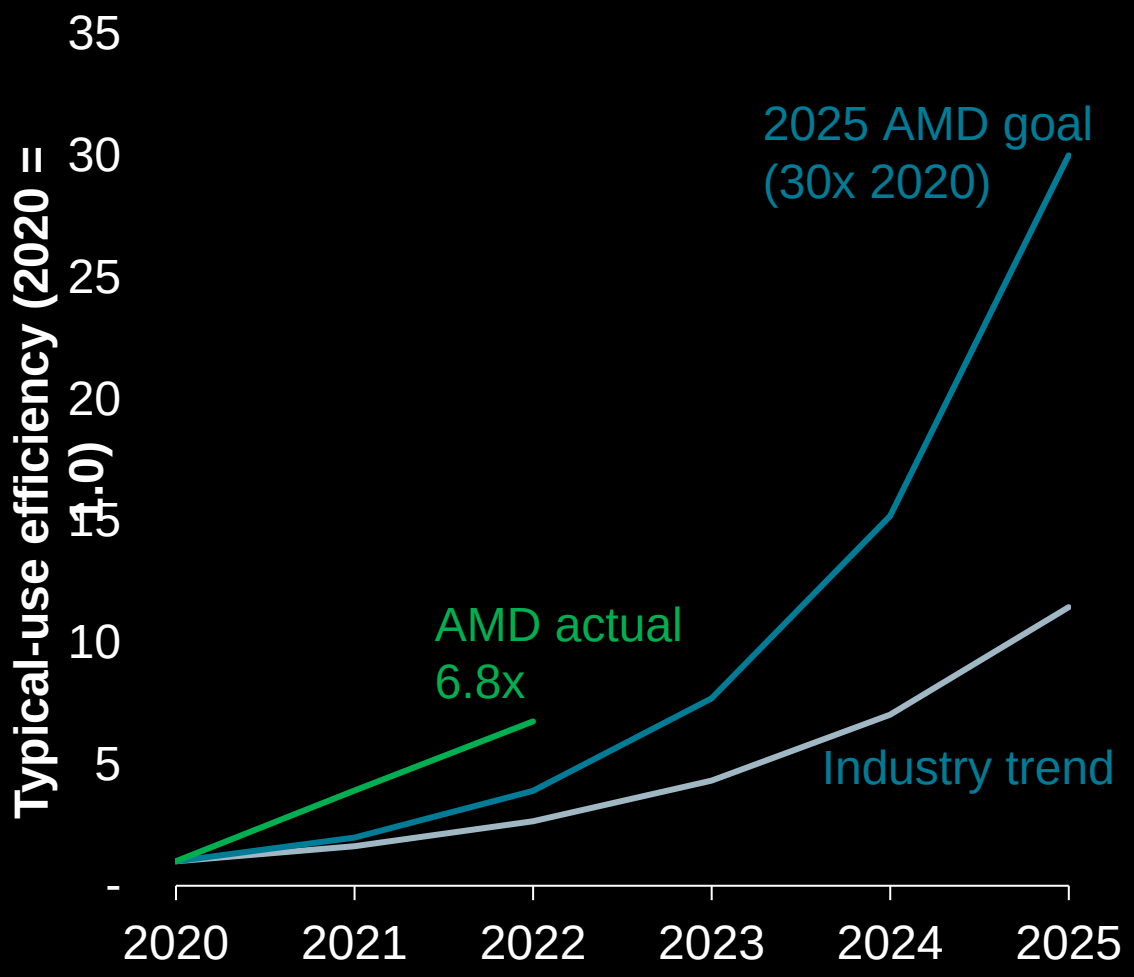
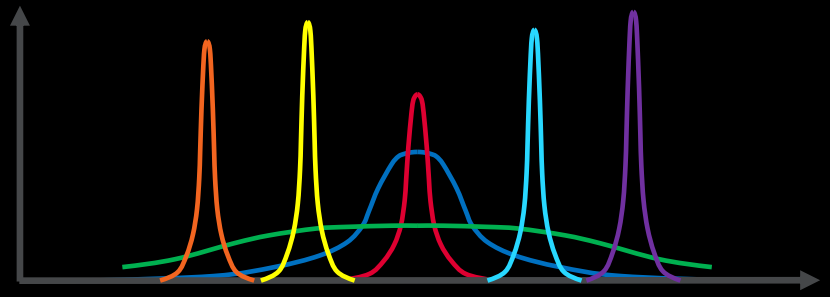
2025 → 2030



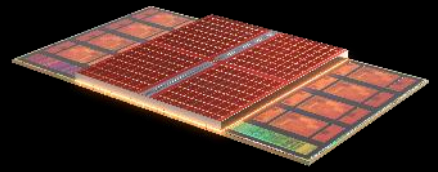
Further application-specific acceleration



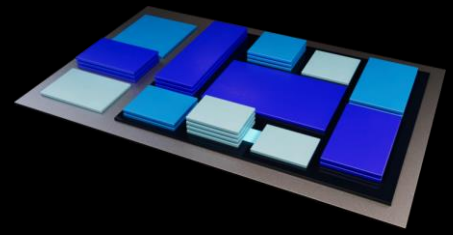
Even more advanced packaging and integration

3D Chiplets → **Next Era for Chiplets**

(Chiplet + Advanced 3D Stacking)



(Multiple combinations of 2D and 3D)



Software and Co-design critical to achieve 1000x

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