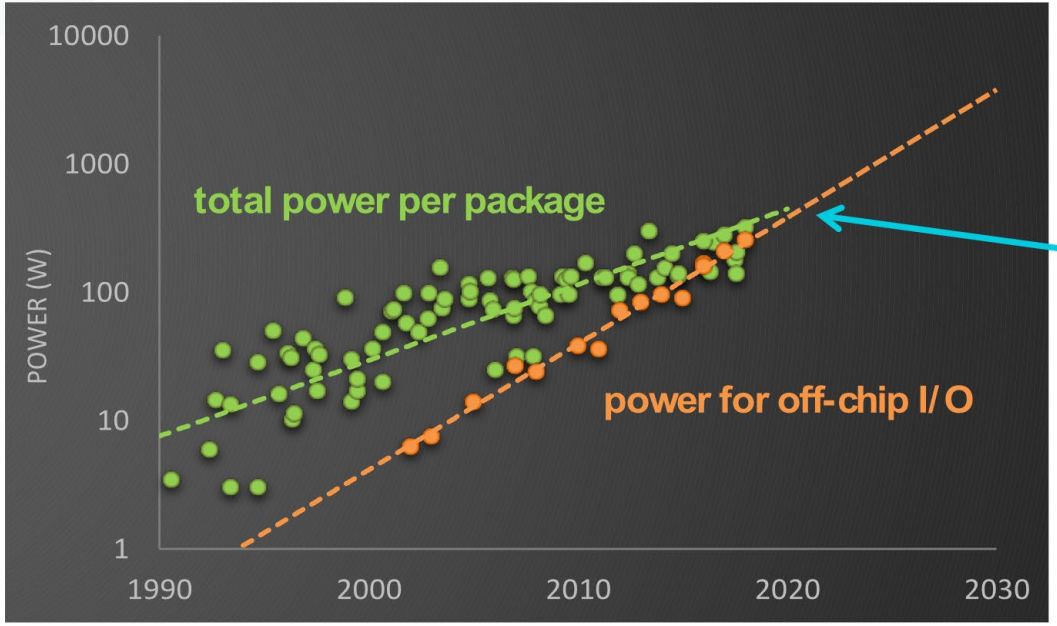
Co-Packaged Optics for Datacenter

E. Jan Vardaman, President and Founder

TechSearch INTERNATIONAL

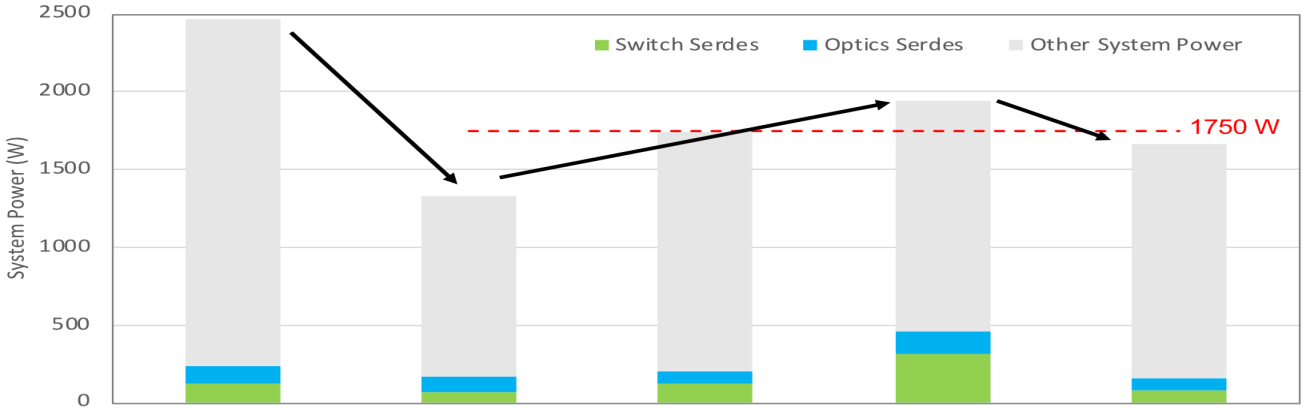
Most Challenging Problems in HPC: I/O Density and Power



[G. Keeler, DARPA ERI 2019]

- As bandwidth increases, energy efficiency per bit decreases, especially for network switch
- Half a chip's power is spent on data transfer (scaling transistors does not solve)
- Power budget is being consumed by electric SERDES interconnect
- Thermal management and total power regulation are also big challenges

Drivers for Co-Packaged Optics at 51.2T



Bandwidth	12.8T	12.8T	25.6T	51.2T	51.2T
Codename	Backpack	Minipack	Minipack 2	Next-Gen	CPO Switch
System Architecture	12 Chip, LR	Single Chip, LR	Single Chip, LR	Single Chip LR	Single Chip, XSR
Optics Form Factor	128 x 100G QSFP-28	128 x 100G QSFP-28	128 x 200G QSFP-56	128 x 400G FPP	CPO

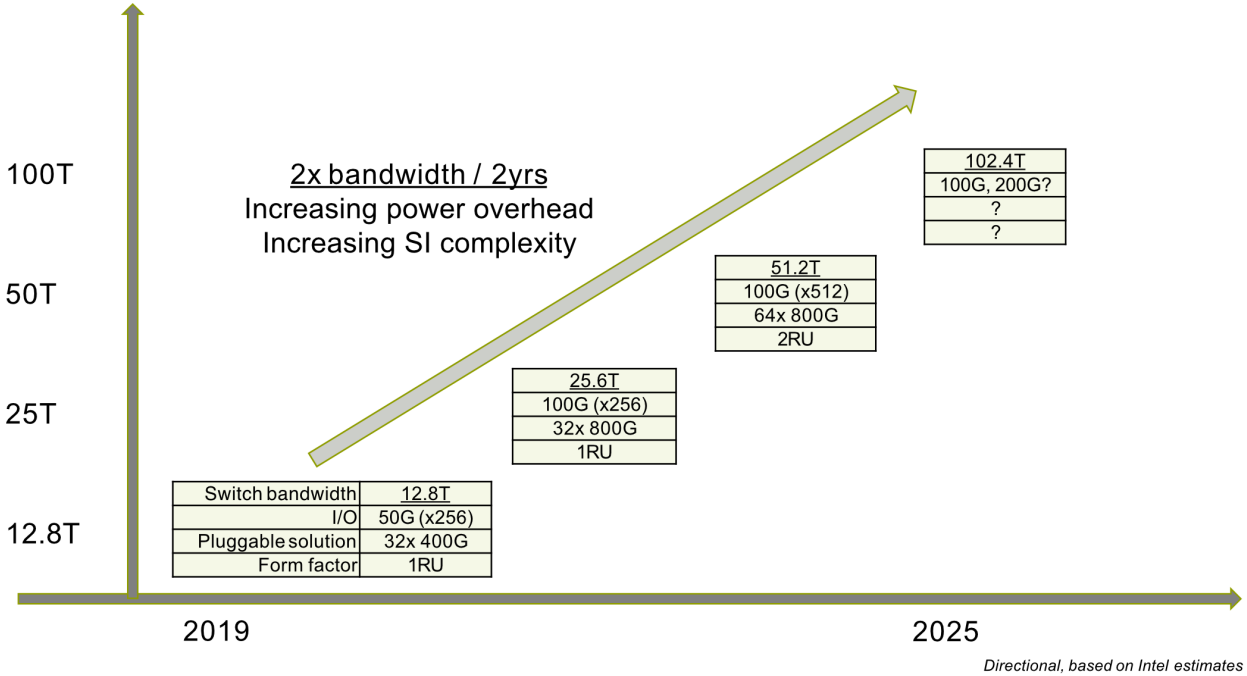
Front-Panel Pluggable Optics

Co-Packaged Optics

Source: IEEE 802.3 Beyond 400G Study Group.

- **Advantages of CPO include improved energy efficiency and bandwidth density, reduced latency, and power efficiency**
- **Adoption of CPO needed for bandwidth at 51.2 Tb/sec**

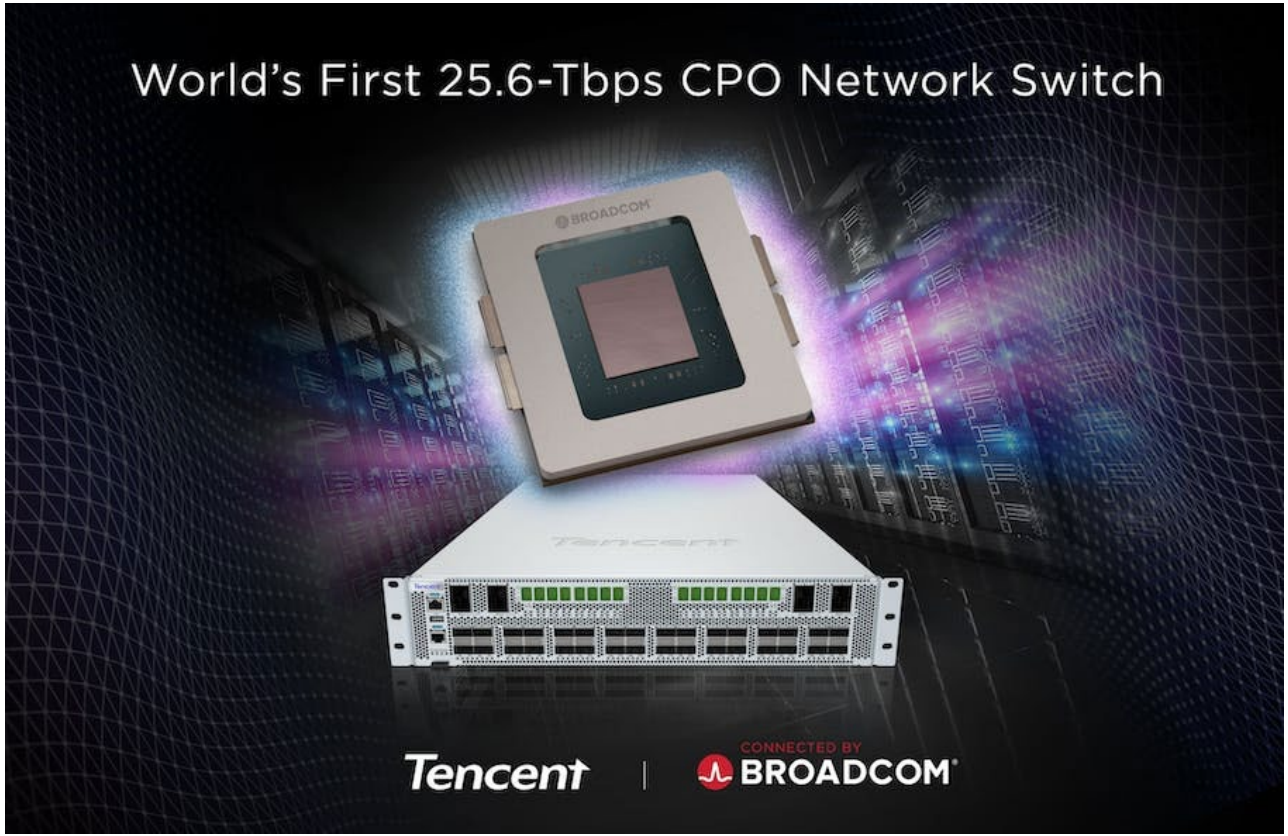
Deployment of Co-Packaged Optics (CPO)



Source: Intel.

- **At 25Tb/s pluggable solutions are deployed and at 51.2Tb/s pluggable optics are still a viable choice, there is value for CPO but supply chain and ecosystem issues are barriers**
- **Intel's 3.2G CPO module is more than 2x density of 2020 demo and 15% greater energy efficiency**
- **AMD was recently issued patent on integration of a photonic and silicon chip on an organic RDL**

CPO for Network Switch for Hyperscale Applications



- **CPO approach enables savings of 30% power and 40% optics cost/bit**

Challenges for Co-Packaged Optics

- **Technical issues are not insurmountable, but integration is the issue**
- **Ecosystem needs to be established, including design capabilities**
  - No standard PDK for Si fab, simulations, or assembly (each company has its own process)
  - Light source has long and expensive development cycle: Co-design of ASIC and Si photonics needed
- **No standardization of module assembly, including fiber light source attach and test**
  - Each product today needs custom assembly infrastructure and processes
- **Need readily, available, and standard components that can be integrated by OSATs and OEM**
  - Need to be able to test and debug
  - Low cost assembly process for high-volume, including fiber attach
- **Innovation in packaging architecture, materials, and processes needed**
  - To enable hybrid optical and electrical interconnect, superior thermal management, and increased total power supply

Thank you!

TechSearch International, Inc.
4801 Spicewood Springs Road, Suite 150
Austin, Texas 78759 USA
+1.512.372.8887
tsi@techsearchinc.com

RELEVANT, ACCURATE, TIMELY