

U.S. DEPARTMENT OF  
**ENERGY**

Office of  
ENERGY EFFICIENCY &  
RENEWABLE ENERGY

# Microelectronics' Energy Efficiency Scaling for 2 Decades (EES2) Pledge and WG WELCOME

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<https://microelectronics.slac.stanford.edu/amo-microelectronics>

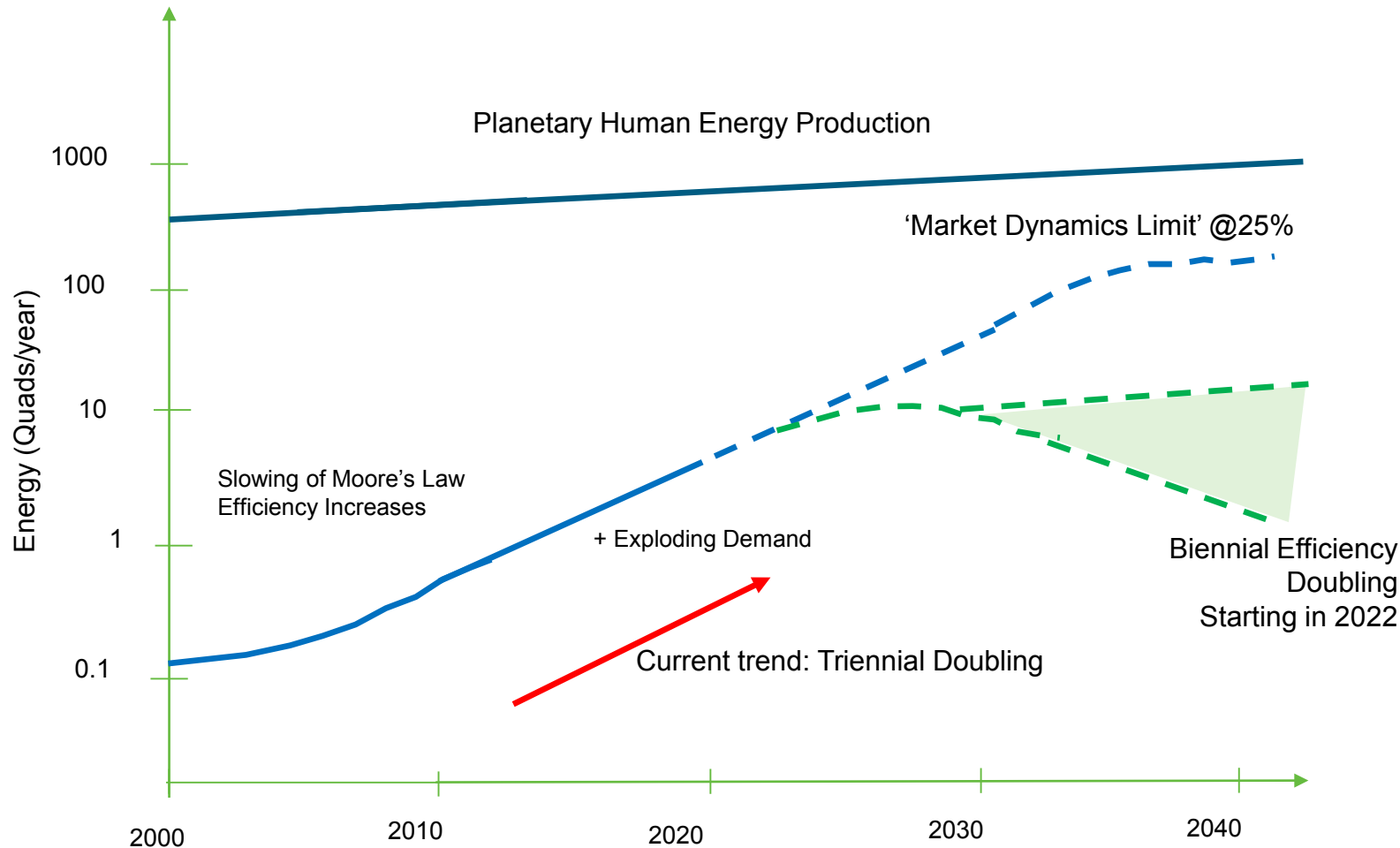


# Recent Events

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- White House supply chain report recommends EES2 (Feb)
- NIST held their own workshops (April)
- CHIPS and Science Act was signed into law. (Aug)
- DOE held EES2 implementation events (Sept) and identified 15 more ideas
- AMO → AMMTO (Oct)

# Background: *Semiconductor Research Corporation Projections vs EES2*



NOTE: log scale on vertical axis

- Era of doubling energy efficiency biennially through planar geometric scaling ended around 2010.
- New application spaces – whose energy use is accelerating (especially AI) are driving increased energy use since 2010. After 2020, electrification adds another fast-doubling driver.
- Depending on demand and implementation, EES2 will flatten or possibly even reduce semiconductor energy use

Source: Based on SRC Decadal Report (2021)

# Why “Scaling” Doubling every two years is needed

Energy Efficiency Scaling for 2 Decades (EES2) –also known as “Green Moore’s Law’ requires efficiency doubling every two years because:

- 1) The PROBLEM is Urgent—hospital computers now shutting down in climate change driven heat waves
- 2) The PROBLEM is rapidly doubling, so too must the solution
- 3) Doubling efficiency every 2 years is what the industry did for 30 generations
- 4) Roughly every two years, there is a new generation of microelectronics, so the goal is synched with the industry’s innovation cycle
- 5) Future Progress in efficiency depends on effective co-design and a specific, technology neutral cross cutting goal requires co-design.



# AMO Semiconductor R&D for Energy Efficiency Series

## KEY TAKEAWAYS

- SRC forecast of unsustainable semiconductor energy use: 25% of planetary energy by 2030
- Data deluge from increased deployment of sensor systems requires minimizing the amount of data created and communicated from the sensor node
- Ultra-energy-efficient (>10X) semiconductor devices to counter trends require ultra-precise manufacturing processes
- Increased industry-government partnerships and access to state-of-the-art facilities for academic and small business researchers to prototype new devices and circuit designs is needed
- Analog and neuromorphic computing approaches and devices can enable efficiency and speed improvements in areas of sensing, communication, and machine learning by >1,000X and potentially 1,000,000 with bio-inspired design
- Advanced packaging is a key first step in integrating advanced technologies in memory, compute, and neuromorphic devices, while improving energy efficiency
- Co-packaged optics (i.e., optical interconnects) may provide up to 10x improvement in efficiency
- 3D hybrid bonding can increase interconnect energy efficiency by 3x and interconnect density by 15x
- **1000X EES2 Goal Announced**

Co-led by DOC National Institute of Standards and Technology (NIST)

Co-sponsored by DOE Office of Science and Semiconductor Research Corporation

Co-led with DOC NIST

### Workshop 1: Integrated Sensor Systems

January 25-26, 2021

### Workshop 2: Ultra-Precise Control for Ultra-Efficient Devices

April 21-23, 2021

### Workshop 3: Mfg. and Integration Challenges for Analog and Neuromorphic Computing

August 11-13, 2021

### Workshop 4: Advanced Packaging for 3D Micro-electronics

January 12-13 /19-20, 2022

# Why Pledge Now

- **Need to Reduce Computing Energy Use has become urgent today**
  - Hospitals shutting down computers to stay cool
  - Cryptocurrency electricity use ??
  - Machine Learning electricity use
- **Energy Efficiency requires top-down and bottom-up efforts (leadership needed to mandate true co-design)**
- **CHIPS and Science Act ->Law**
  - Good Opportunity to get Semiconductor Industry Leadership Attention!!!



# EES2 Goal Cooperation Pledgers—Sept 20



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## We the undersigned agree to cooperate

- To identify and publicize problems solved and the opportunities offered by microelectronics' Energy Efficiency Scaling over the next 2 Decades (EES2),
- To participate in the AMO-led EES2 2022-2023 R&D Roadmapping effort, and
- To explore formation of a partnership a "EES2 Alliance" that enables the EES2 1000X efficiency increase goal by leading EES2 RDD&D Roadmapping after 2023 and by catalyzing the deployment of cost-effective technologies needed to stay on the EES2 path of doubling microelectronics' energy efficiency every two years.

## We do this because

- Microelectronics' life-cycle energy use is rapidly becoming unsustainable.
- EES2 is a key organizing principle that also counters this energy use.
- The EES2 is a technology leadership path that provides economic and other public benefits.



alignedcarbon





# EES2 Pledgers & Expanded Pledge –Nov 16



## We the undersigned agree to cooperate

- To document and learn from the extraordinary record of microelectronics', including power electronics', energy efficiency such as increases greater than 1,000,000x in energy efficiency since the invention of the transistor nearly 75 years ago;
- To document and learn from microelectronics' past and forecasted future ability to enable all sectors of the economy to become more energy efficient and sustainable;
- To identify and publicize problems solved and opportunities offered by microelectronics' Energy Efficiency Scaling over 2 Decades (EES2);
- To participate in the AMO-led EES2 2022-2023 R&D roadmapping effort; and
- To explore formation of a partnership, an "EES2 Alliance" that enables the EES2 1000X efficiency increase goal by leading EES2 R&D Roadmapping after 2023 and by catalyzing the deployment of cost-effective technologies, including power electronics, needed to stay on the EES2 path of doubling microelectronics' energy efficiency every two years.

## We do this because

- Microelectronics' life-cycle energy use is rapidly becoming unsustainable as microelectronics demand begins to outpace continuing efficiency improvements due to burgeoning computing, communication, and electrification demands
- EES2 is a key organizing principle that aims to help meet new energy demands
- The EES2 is a technology leadership path that provides economic and other public benefits.





# EES2 Working Groups must first Identify Most Urgent Problems

## For example, EES2 Goal Technology Solutions must address:

- **Energy efficiency increases from miniaturization are slowing down**
  - Time between successive technology nodes are extending
  - Miniaturization doesn't reduce energy use (as much) due to 'leakage'
  - Sub 10nm node chips' severe thermal management issues.
- **Energy demand of microelectronics is accelerating most in key areas**
  - Cryptocurrency now doubles energy use every 2 years.
  - Certain ML programs double energy use every 2-3 months.
  - Non-computing communications applications now > computing.
  - Electrification for decarbonization will further increase demand (e.g. 65x for EVs)



**Thank you**

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