U.S. DEPARTMENT OF
ENERGY

Office of
ENERGY EFFICIENCY & RENEWABLE ENERGY

ADVANCED MATERIALS & MANUFACTURING TECHNOLOGIES OFFICE

Welcome to EES2 and FINAL Roadmap Working Group Meeting #9

Tina Kaarsberg, PhD
EES2 Workshop Co-Chair

August 16, 2023

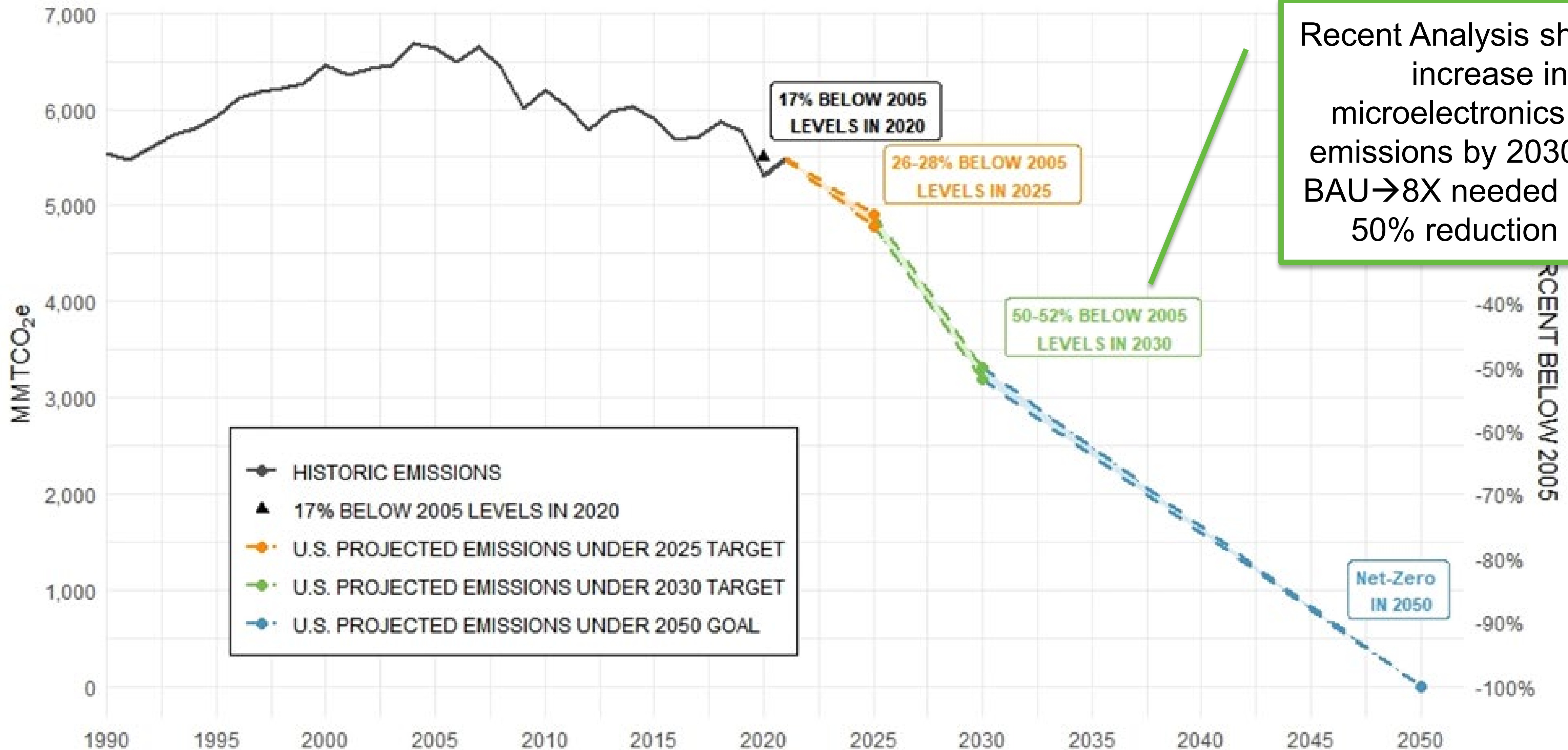
https://microelectronics.slac.stanford.edu/amo-microelectronics

Climate Change: Code RED for Humanity

Last month was the hottest month ever recorded for the planet, this month showed more extreme weather impacts

Maui Wildfires

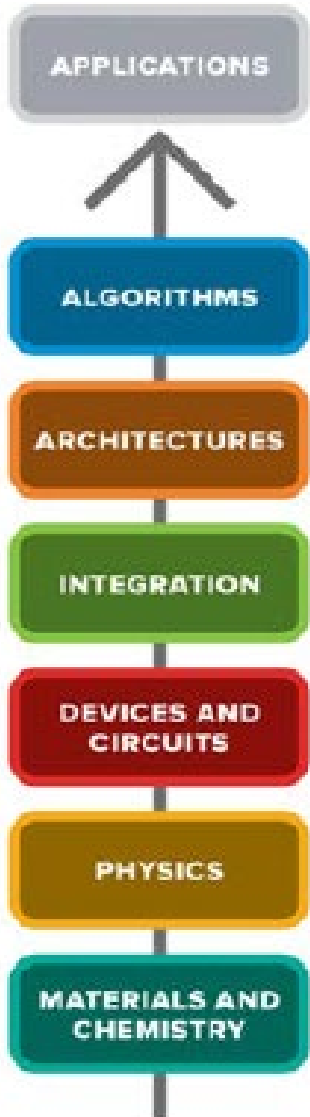
US International Agreements on GHG Reductions



Recent Analysis shows 4X increase in microelectronics GHG emissions by 2030 under BAU→8X needed to meet 50% reduction goal

From Whitehouse.gov Jan 2021 Report

"Stack" →EES2 Roadmap's Working Groups



Stack

- Algorithms /Software
- Heterogenous Integration and Advanced Packaging
- Circuits and Architectures
- Materials and Devices

PLUS

- Metrology and Benchmarking
- Power and Control Electronics
- Manufacturing Energy Efficiency and Sustainability

Under EES2, Microelectronics is doing its part by 2030

10X efficiency increase implies 10X reduction in associated GHG emissions

Efficiency Increase

1000x

100x

10x

Deploy in 0 to 7 years commercial & recently demonstrated technologies using Best Practices, Voluntary Standards. Basic, applied R&D, demonstrations all start in year 1.

Deploy in 7 to 13 years by commercialization of Applied R&D started in year 1. Begin Applied R&D on Basic R&D started in year 1

Deploy in 13 to 20 years by commercialization of applied R&D from basic research started in year 1

2030 and 2036 goals differentiate EES2 from other 100X goals

2030 2036 2043 2050?

Year

AMMTO intends to support 10x Wedge from MnD

Efficiency

1000x

100x

10x

2023 Lab Call for 10X efficient Devices—1 award in 2023, potential addt'l awards in 2024

Sandia National Laboratories

2030

Yea
r

2036

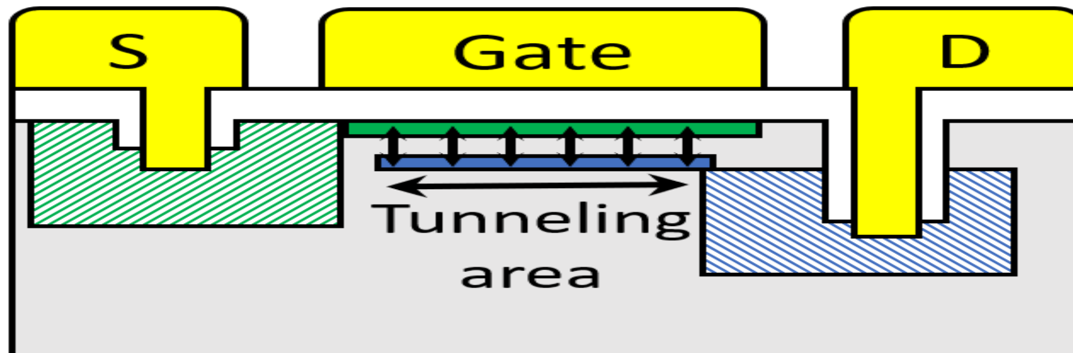
2043

Today's Announcement: 1st EES2 R&D Award

a 10X Energy Efficient vTFET to replace MOSFET

Technology Summary

Project will experimentally and theoretical verify energy efficiency and speed of a silicon vertical tunnel field effect transistor (vTFET) made using atomic precision advanced manufacturing (APAM). The vTFET reduces the voltage compared to conventional microelectronic transistors by 3X (see figure at right), leading to 10X improvement in fJ/switch. Design leverages the atomically abrupt doping profiles and record-breaking dopant densities achieved by APAM, which also enables the vertical geometry that increases current.

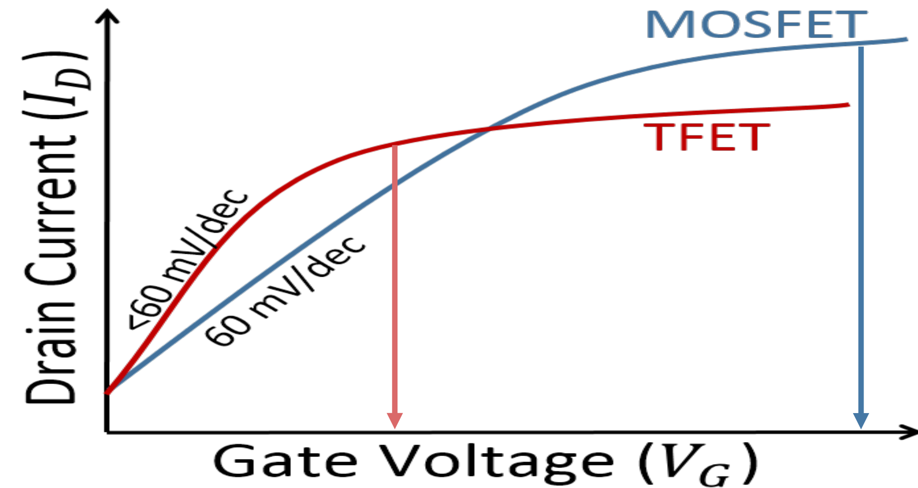


Deliverables

36 months; Federal funding $4M

Year 1	-Create experimental & modeling platforms
Year 2	-Measure tunneling devices with combinations of gated layers, commercial epi, and APAM epi -Create multi-scale model based on real devices
Year 3	-Demo real vTFET and simulate energy eff. -Contrast commercial and APAM epi for vTFET

Key Performance Metric



3X reduced voltage → 10X reduced power consumed by entire processor

Technology Commercialization Strategy

In addition to demonstrating the vTFET, Sandia will build a multi-scale modeling framework, based on real devices, that includes the quantum mechanics of tunneling and enables optimizations to include cost-lowering and performance enhancing features only available to industry. Combined with experimentation on the differences between APAM-based and conventional epitaxy-based devices, Sandia's project will provide industry with the motivation and tools to deploy the vTFET as a 10X energy efficient, general purpose, CMOS-compatible, drop-in alternative to MOSFET. **To increase likelihood of industry uptake, Sandia is seeking members for an Industrial Advisory Board.**

10x energy efficiency in general purpose, Si-based transistors

And There's More!

Preliminary Version for WG Review

WG Results Table to be included in NIST MAPT!

Working Group	Energy Efficiency Technology	Near Term (0-5yrs)	Mid Term (5-10 yrs)	Long Term (10+ yrs)
Materials and Devices	Key Energy Efficient Technologies	**CNTFET (logic)**	**TFET**	**Analog devices for neuromorphic**
	Key Challenges	• Production of pristine and near-pure population of CNTs. • Reducing CNT contact resistance.	• Fabrication of consistent tunnel junction. Currently, variability is high. • Demonstration of high on/off ratio and low voltage operation.	• Down-selecting from a wide breadth of materials, designs, and approaches that fit need. • Performance loss during integration with conventional technologies.
Circuits and Architectures	Key Energy Efficient Technologies	**Domain Specific Architectures**	**EDA**	**Compute in Memory**
	Key Challenges	• Architecture is set up after software • ASICs are not adaptable to other systems	• Simulation of device function is limited • 3D stacked technologies are lacking	• Technology is available, however software difficulties are preventing integration
Advanced Packaging and Heterogeneous Integration	Key Energy Efficient Technologies	**Advanced Thermal Interface Materials**	**CNT Global Interconects**	**Monolithic Integration**
	Key Challenges	• Thermal resistance at interfaces is poorly understood • CTE material mismatch can cause cracking and lowering heat removal	• Contact resistance between CNT/Metal is high and poorly understood • Deposition methods for vertical CNT's require high temperatures which may not be BEOL compatible	• Thermal management during operation • Higher tiered technology has lower performance due to thermal budget constraints

Still More!

Preliminary Version for WG Review

WG Results Table to be included in NIST MAPT!

Working Group	Energy Efficiency Technology	Near Term (0-5yrs)	Mid Term (5-10 yrs)	Long Term (10+ yrs)
Software and Algorithms	Key Energy Efficient Technologies	**Resource-Aware Workload Scheduling**	**Improved Training Algorithms**	**Optimization of memory access in algorithms**
	Key Challenges	• Scheduling work both temporally and spatially • Near-real-time resource availability disseminated to participating nodes	• Achieving continual/sequential learning • Data/dimensional reduction and specificity	• Optimization depends on architecture • Software compatibility
Power and Control Electronics	Key Energy Efficient Technologies	End-to-end power delivery for data centers	Use of wide bandgap power devices and optimized technologies	Power deliery for photonic integrated circuits

Metrology Technology Approach	Challenges
All metrology	• Bridging the gap between idealized system metrology and actual system performance. • Dearth of samples to develop new metrology techniques. • Avoid excessive measurements, understanding process dependency to capture only what's necessary.
3D metrology (thermal, interface, etc.)	• Inability to evaluate properties of interest at inaccessible points within 3D structures without typically resorting to destructive techniques. • Very large data sets from 3D metrology – hard to manage.
Material property measurements, including thin film and patterned materials	• Inaccuracy of material and interface properties that are used in computational models of 3D structures. • Most material property measurements based on bulk materials, when using these materials in real systems, they are at micro/nano scales (i.e., thin films) where material properties are different.