U.S. DEPARTMENT OF ENERGY

Office of ENERGY EFFICIENCY & RENEWABLE ENERGY

Microelectronics' Energy Efficiency Scaling for 2 Decades (EES2) Pledge and WG

WELCOME to Day 2

Tina Kaarsberg, PhD

EES2 Workshop Co-Chair

Advanced Materials and Manufacturing Technology Office (AMMTO)

March 16, 2023

https://microelectronics.slac.stanford.edu/amo-microelectronics

ORIGINAL EES2 GOAL—Jan 12, 2022—no *addition needed??*

Shift from R&D Roadmaps based on biennial length-based scaling (e.g., Moore's law) to ultra-energy-efficiency scaling and ensure all R&D includes some energy-efficiency focus

- Specifically, develop in partnership with U.S. and Allied Country Semiconductor Industry an RDD&D roadmap to ensure
  - **Doubling* of microelectronics' energy efficiency every two years *or faster* for the coming decades**
    - ***that doubling be ABOVE/Beyond miniaturization-based energy efficiency doubling that is still happening every 2.5->3 years***
  - **In two decades, increase energy efficiency of next generation microelectronics by >1000X**

DOE Semiconductor R&D for Energy Efficiency Series

https://microelectronics.slac.stanford.edu/amo-semiconductors

KEY TAKEAWAYs

Workshop 1: Integrated Sensor Systems
January 25-26, 2021

- SRC forecast of unsustainable semiconductor energy use: 25% of planetary energy by 2030
- Data deluge from increased deployment of sensor systems requires minimizing the amount of data created and communicated from the sensor node

Workshop 2: Ultra-Precise Control for Ultra-Efficient Devices
April 21-23, 2021

- Ultra-energy-efficient (>10X) semiconductor devices to counter trends require ultra-precise manufacturing processes
- Increased industry-government partnerships and access to state-of-the-art facilities for academic and small business researchers to prototype new devices and circuit designs is needed

Co-led by DOC National Institute of Standards and Technology (NIST)

Workshop 3: Mfg. and Integration Challenges for Analog and Neuromorphic Computing
August 11-13, 2021

- Analog and neuromorphic computing approaches and devices can enable efficiency and speed improvements in areas of sensing, communication, and machine learning by >1,000X and potentially 1,000,000 with bio-inspired design
- Advanced packaging is a key first step in integrating advanced technologies in memory, compute, and neuromorphic devices, while improving energy efficiency

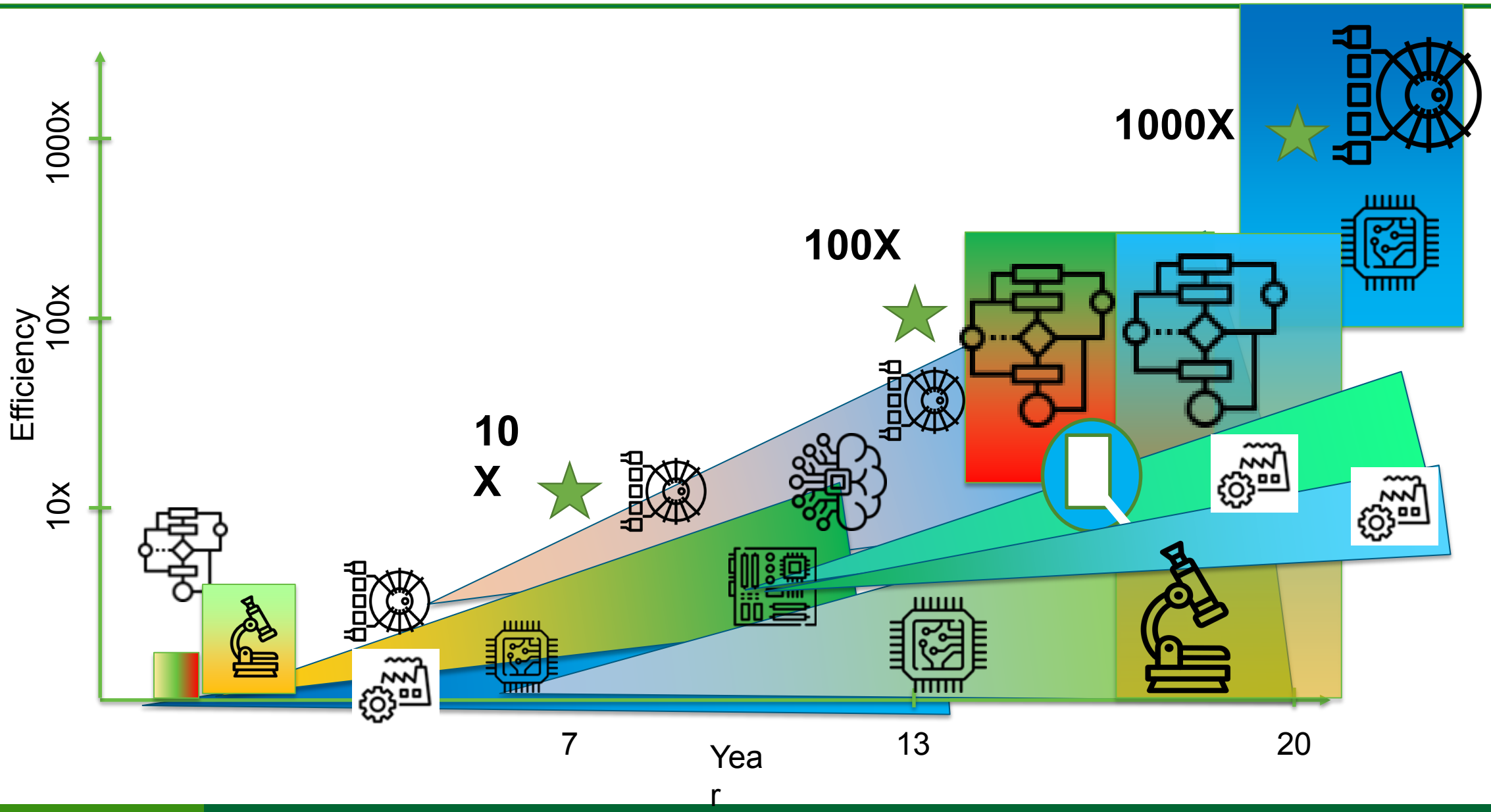
Co-sponsored by DOE Office of Science and Semiconductor Research Corporation

Workshop 4: Advanced Packaging for 3D Micro-electronics
January 12-13 /19-20, 2022

- Co-packaged optics (i.e., optical interconnects) may provide up to 10x improvement in efficiency
- 3D hybrid bonding can increase interconnect energy efficiency by 3x and interconnect density by 15x
- **1000X EES2 Goal Announced**

Co-led with DOC NIST

Tech Deployment Scenario for doubling every 2 years +Gr +Blue



Next Steps: Go Back to Pledge as our Guide

We the undersigned agree to cooperate

- To document and learn from the extraordinary record of microelectronics', including power electronics', energy efficiency such as increases greater than 1,000,000x in energy efficiency since the invention of the transistor nearly 75 years ago;
- To document and learn from microelectronics' past and forecasted future ability to enable all sectors of the economy to become more energy efficient and sustainable;
- To identify and publicize problems solved and opportunities offered by microelectronics' Energy Efficiency Scaling over 2 Decades (EES2);
- To participate in the AMMTO-led EES2 2022-2023 R&D roadmapping effort; and
- To explore formation of a partnership, an "EES2 Alliance" that enables the EES2 1000X efficiency increase goal by leading EES2 R&D Roadmapping after 2023 and by catalyzing the deployment of cost-effective technologies, including power electronics, needed to stay on the EES2 path of doubling microelectronics' energy efficiency every two years.

We do this because

- Microelectronics' life-cycle energy use is rapidly becoming unsustainable as microelectronics demand begins to outpace continuing efficiency improvements due to burgeoning computing, communication, and electrification demands
- EES2 is a key organizing principle that aims to help meet new energy demands
- The EES2 is a technology leadership path that provides economic and other public benefits.

Next Steps To Do List for Non-R&D Roadmap Part of Pledge

- More, Better Data on Microelectronics Energy Use (EIA, DOC)
- Publicize Sadas' Findings
- Pick a Logo
- Summer Meeting of Sr. Pledge Officials on Outreach'
- Get Briefings from Sadas' Postdocs

Thank you

Tina.Kaarsberg@ee.doe.gov

For office information and to subscribe for updates:

manufacturing.energy.gov