

U.S. DEPARTMENT OF  
**ENERGY**

Office of  
ENERGY EFFICIENCY &  
RENEWABLE ENERGY

# Microelectronics' Energy Efficiency Scaling for 2 Decades (EES2) Pledge and WG WELCOME

**Tina Kaarsberg, PhD**

**EES2 Workshop Co-Chair**

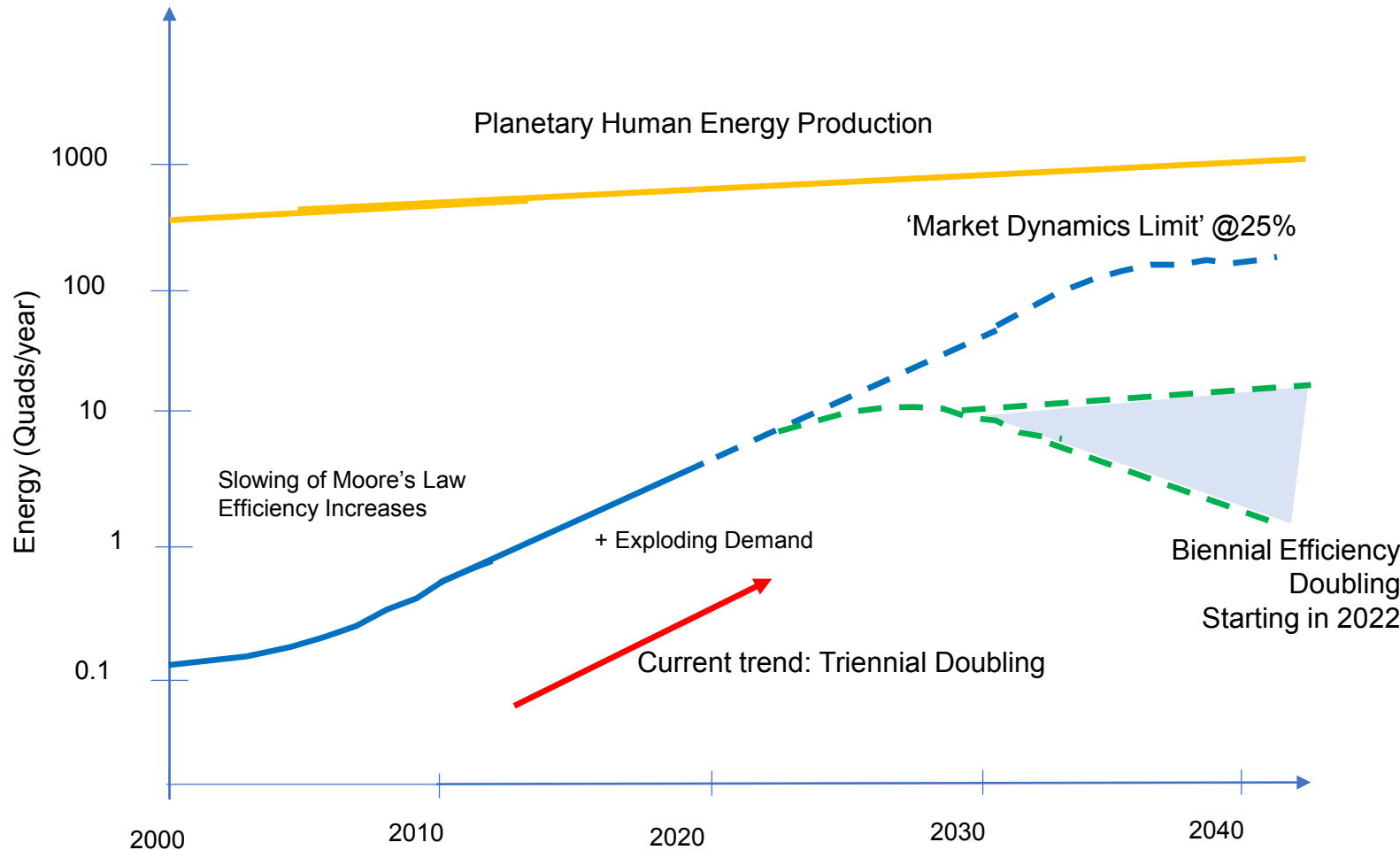
Advanced Materials and Manufacturing Technology Office (AMMTO)

January 12, 2023

<https://microelectronics.slac.stanford.edu/amo-microelectronics>



# *Semiconductor Research Corporation Projections vs EES2*



NOTE: log scale on vertical axis

- Era of doubling energy efficiency biennially through planar geometric scaling ended around 2010.
- New application spaces –whose energy use is accelerating (especially AI) are driving increased energy use since 2010. After 2020, electrification adds another fast-doubling driver.
- Depending on demand and implementation, EES2 will flatten or possibly even reduce semiconductor energy use

Source: Based on SRC Decadal Report (2021)

# Why “Scaling” Doubling every two years is needed

Energy Efficiency Scaling for 2 Decades (EES2) –also known as “Green Moore’s Law’ requires efficiency doubling every two years because.

- 1) PROBLEM is Urgent—climate-driven extreme weather stresses electricity supply
- 2) The PROBLEM is rapidly doubling, so too must the solution
- 3) Doubling efficiency every 2 years is what the industry did for 30 generations
- 4) Every two years there is a new generation of microelectronics so the goal is synched with the industry’s innovation cycle
- 5) **Future Progress in efficiency depends on effective co-design and a specific, technology neutral cross cutting goal**



# DOE Semiconductor R&D for Energy Efficiency Series

<https://microelectronics.slac.stanford.edu/amo-semiconductors>

## KEY TAKEAWAYS

- SRC forecast of unsustainable semiconductor energy use: 25% of planetary energy by 2030
- Data deluge from increased deployment of sensor systems requires minimizing the amount of data created and communicated from the sensor node
- Ultra-energy-efficient (>10X) semiconductor devices to counter trends require ultra-precise manufacturing processes
- Increased industry-government partnerships and access to state-of-the-art facilities for academic and small business researchers to prototype new devices and circuit designs is needed
- Analog and neuromorphic computing approaches and devices can enable efficiency and speed improvements in areas of sensing, communication, and machine learning by >1,000X and potentially 1,000,000 with bio-inspired design
- Advanced packaging is a key first step in integrating advanced technologies in memory, compute, and neuromorphic devices, while improving energy efficiency
- Co-packaged optics (i.e., optical interconnects) may provide up to 10x improvement in efficiency
- 3D hybrid bonding can increase interconnect energy efficiency by 3x and interconnect density by 15x
- **1000X EES2 Goal Announced**

Co-led by DOC National Institute of Standards and Technology (NIST)

Co-sponsored by DOE Office of Science and Semiconductor Research Corporation

Co-led with DOC NIST

### Workshop 1: Integrated Sensor Systems

January 25-26, 2021

### Workshop 2: Ultra-Precise Control for Ultra-Efficient Devices

April 21-23, 2021

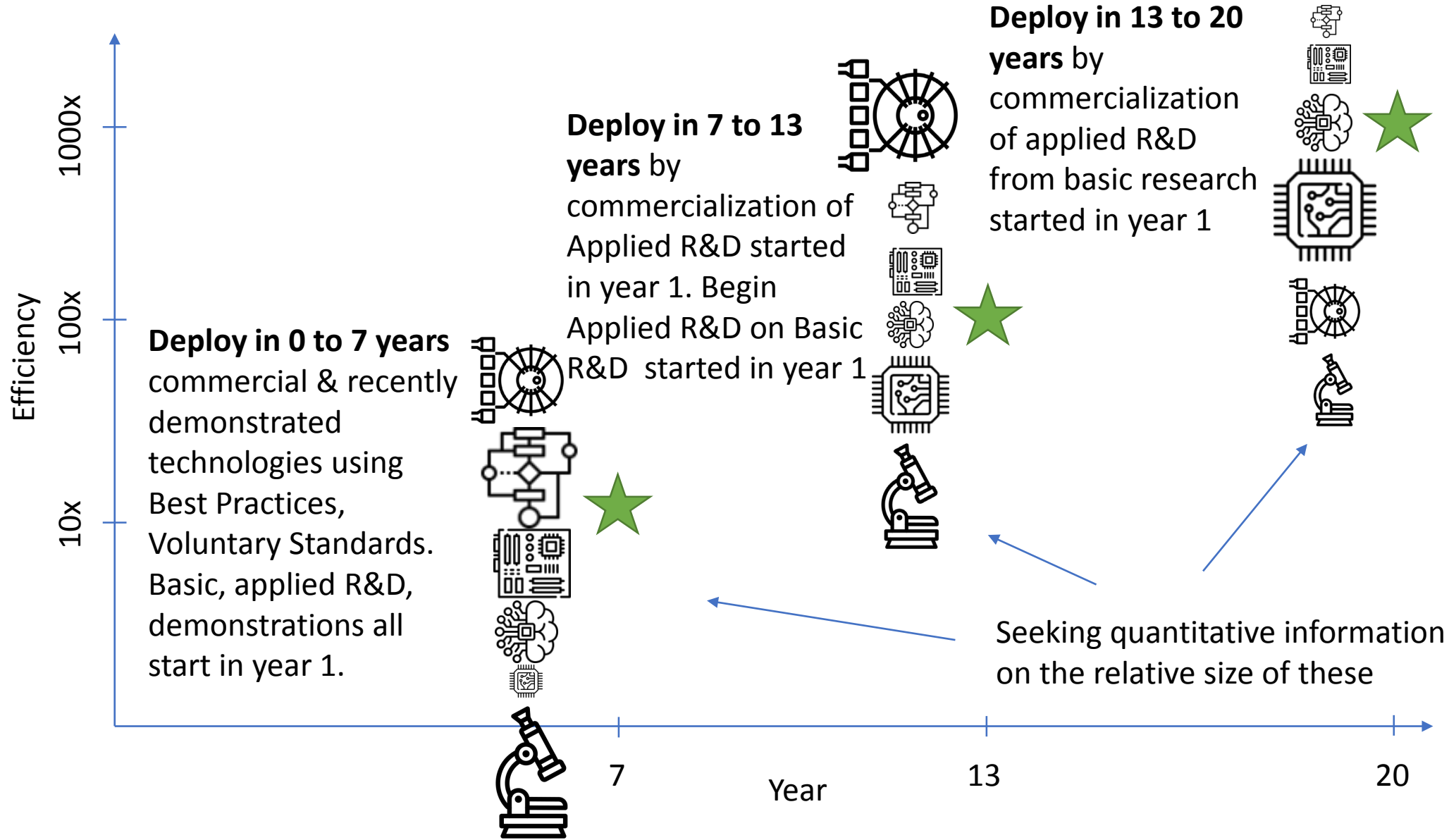
### Workshop 3: Mfg. and Integration Challenges for Analog and Neuromorphic Computing

August 11-13, 2021

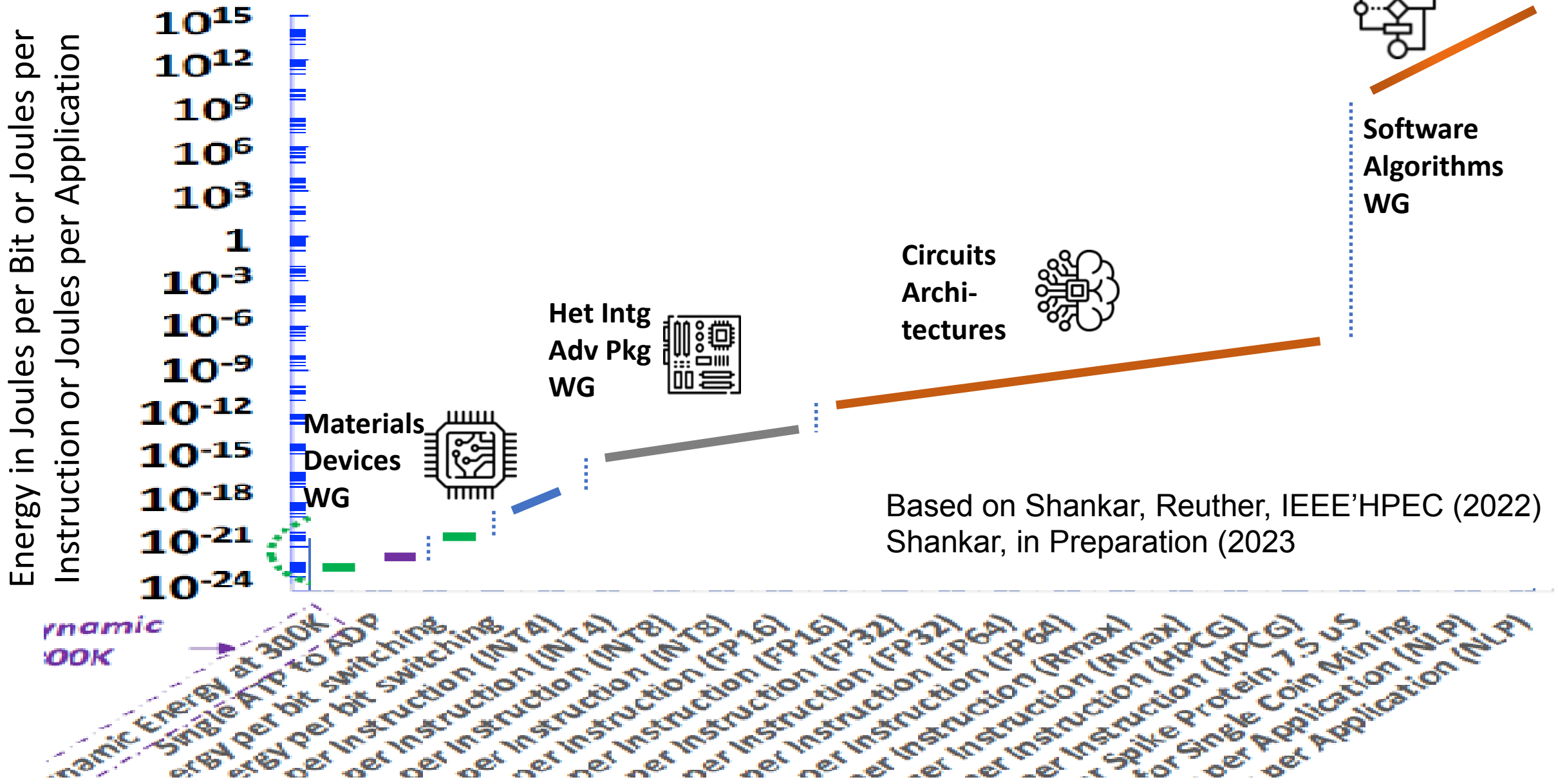
### Workshop 4: Advanced Packaging for 3D Micro-electronics

January 12-13 /19-20, 2022

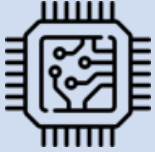

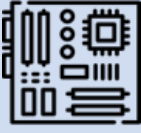

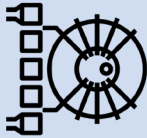


# Tech Deployment Scenario for doubling every 2 years



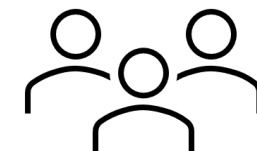
# Simplified slide on energy Use for different Layers of Computing



# EES2 Working Group Homework **Today**

	Materials and Devices	Circuits and Architectures	Het Intg Adv Pkg	Metrology & Benchmark	Power & Control	Software Algorithms	Mfg Energy Efficiency
Working Group							
Co-chair Point for February 2023	John Doe, XYZ Lab	Jane Doe, XYZ Inc.	Raj Doe, ABC Inc.	Dong Doe, ABC Lab	Mo Doe, 123 Inc.	Melinda Doe, MLM Corp.	Cochairs TBD by Feb.
Working Group Highlight Month	March	April	May	<b>February</b>	June	July	August

...don't, stop, thinking about the Workforce





# Why Even MORE Urgency (to get Roadmap done and get more Pledgers)!

- Sadas Analysis shows huge gaps from Energy per bit, per instruction, and per application (especially AI!!) → and gaps seem to be growing
- Broadening the EES2 Community will get us to convince participants with blind spots (e.g. AI) to join
- CHIPS and Science Act ->Law
  - Working with the DOE on Efficiency NOW is a great opportunity to get Attention of NIST, DOD and NSF.





**Thank you**

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**For office information and to subscribe for updates:**

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