U.S. DEPARTMENT OF ENERGY
Office of ENERGY EFFICIENCY & RENEWABLE ENERGY

Microelectronics' Energy Efficiency Scaling for 2 Decades (EES2) Pledge and WG WELCOME to Day 2

Tina Kaarsberg, PhD

EES2 Workshop Co-Chair

Advanced Materials and Manufacturing Technology Office (AMMTO)

January 12, 2023

https://microelectronics.slac.stanford.edu/amo-microelectronics

KILOWATTHOURS

DOE Semiconductor R&D for Energy Efficiency Series

https://microelectronics.slac.stanford.edu/amo-semiconductors

KEY TAKEAWAYs

Workshop 1: Integrated Sensor Systems
January 25-26, 2021

- SRC forecast of unsustainable semiconductor energy use: 25% of planetary energy by 2030
- Data deluge from increased deployment of sensor systems requires minimizing the amount of data created and communicated from the sensor node

Workshop 2: Ultra-Precise Control for Ultra-Efficient Devices
April 21-23, 2021

- Ultra-energy-efficient (>10X) semiconductor devices to counter trends require ultra-precise manufacturing processes
- Increased industry-government partnerships and access to state-of-the-art facilities for academic and small business researchers to prototype new devices and circuit designs is needed

Co-led by DOC National Institute of Standards and Technology (NIST)

Workshop 3: Mfg. and Integration Challenges for Analog and Neuromorphic Computing
August 11-13, 2021

- Analog and neuromorphic computing approaches and devices can enable efficiency and speed improvements in areas of sensing, communication, and machine learning by >1,000X and potentially 1,000,000 with bio-inspired design
- Advanced packaging is a key first step in integrating advanced technologies in memory, compute, and neuromorphic devices, while improving energy efficiency

Co-sponsored by DOE Office of Science and Semiconductor Research Corporation

Workshop 4: Advanced Packaging for 3D Micro-electronics
January 12-13 /19-20, 2022

- Co-packaged optics (i.e., optical interconnects) may provide up to 10x improvement in efficiency
- 3D hybrid bonding can increase interconnect energy efficiency by 3x and interconnect density by 15x
- **1000X EES2 Goal Announced**

Co-led with DOC NIST

ORIGINAL EES2 GOAL—Jan 12, 2022—still the same

Shift from R&D Roadmaps based on biennial length-based scaling (e.g., Moore's law) to ultra-energy-efficiency scaling and ensure all R&D includes some energy-efficiency focus

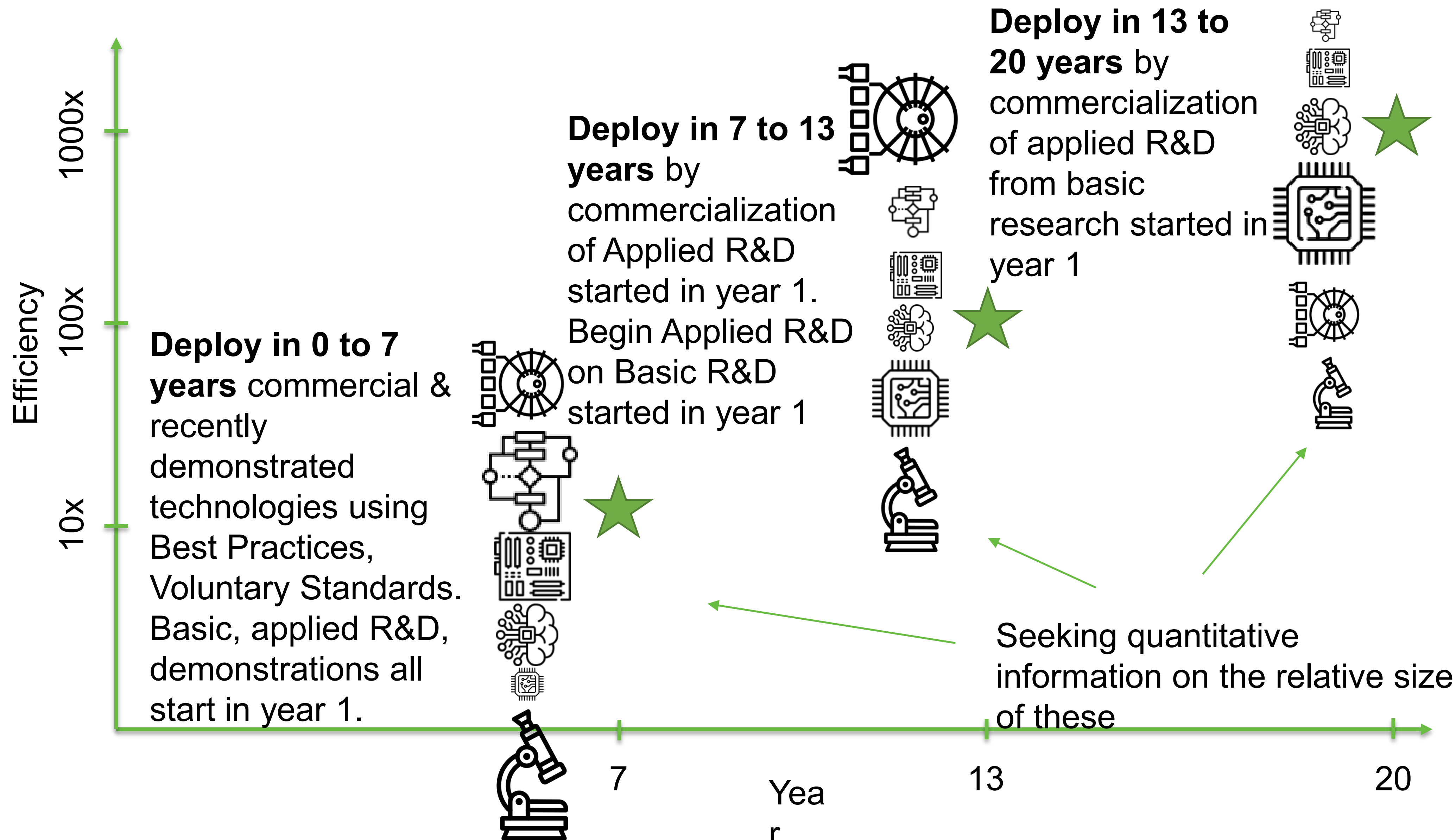
- Specifically, develop in partnership with U.S. and Allied Country Semiconductor Industry an RDD&D roadmap to ensure
  - **Doubling of microelectronics' energy efficiency every two years or faster for the coming decades**
  - **In two decades, increase energy efficiency of next generation microelectronics by >1000X**

Why "Scaling" Doubling every two years is needed

Energy Efficiency Scaling for 2 Decades (EES2) –also known as "Green Moore's Law' requires efficiency doubling every two years because.

1) PROBLEM is Urgent—climate-driven extreme weather stresses electricity supply
2) The PROBLEM is rapidly doubling, so too must the solution
3) Doubling efficiency every 2 years is what the industry did for 30 generations
4) Every two years is there is a new generation of microelectronics so the goal is synched with the industry's innovation cycle
5) Future Progress in efficiency depends on effective co-design and a specific, technology neutral cross cutting goal

Tech Deployment Scenario for doubling every 2 years



Thank you

Tina.Kaarsberg@ee.doe.gov

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