U.S. DEPARTMENT OF ENERGY

Office of ENERGY EFFICIENCY & RENEWABLE ENERGY

ADVANCED MATERIALS & MANUFACTURING TECHNOLOGIES OFFICE

EES2 ENERGY EFFICIENCY SCALING

Day 2 Opening EES2 Workshop and Final V 1.0 Roadmap WG Meeting (#9)

Tina Kaarsberg, PhD
EES2 Workshop Co-Chair

August 17, 2023

https://microelectronics.slac.stanford.edu/amo-microelectronics

Overview

Announcements/Updates

- AMMTO Power Electronics
- New EES2 Education Workforce Development Goal
- Proposed Roadmap Chapters (1 per Working Group + intro and EWD)

Continuation of To do from Yesterday

– *Proposed Roadmap WG/ Tech Boxes/Highlights (based on presentations)*

– *Publications/ Blogs*

– *EES2 Secretariat Activities (Recruitment (Yay Fermilab!) –esp. academia 4 new goal) new Webpage, Wikipedia, Book Club)*

AMMTO Power Electronics (Roadmap & PowerAmerica)

Paul Syers, former EES2 co-chair, now to lead AMMTO Power Electronics:

- AMMTO Power Electronics Roadmap

WG Chair: **Andrew Binder**	• Materials & active components	**Lead:** Sandia National Laboratories
WG Chair: **Faisal Khan**	• Reactive & passive components and packaging	**Lead:** NREL
WG Chair: **Jack Flicker**	• System-level design (e.g., functionality & topology) • Application-specific opportunities	**Lead:** Sandia National Laboratories
WG Chair: **Sam Reese**	• LCA for the power electronics value chain	**Lead:** NREL

Analysis measurement & characterization (cross-cutting)

Lead: Lawrence Livermore National Laboratory

PowerAmerica

1st ManufacturingUSA Consortium

Launched: 2014, federal funding ended in 2020
Lead: North Carolina State University
Current Number of Members: 82
Past Federal Funding: $70 Million
Cost share: ~$75 Million

New EES2 Education Workforce Development Goal

- Within a Decade, **to dramatically increase** the pool of semiconductor-interested STEM students for the electronics engineering and related workforce.

- Partner with BRDG, SRC, SEMI

- Especially from First in Family and other Underrepresented Groups (women should be majority!)

- Measure by getting redoing the survey they did for https://www.imeche.org/policy-and-press/reports/detail/five-tribes-personalising-engineering-education

BRDG
bridge to connect

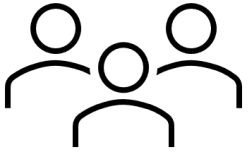
Revision of EES2 Roadmap Chapters (Draft)

1. Introduction and Overview
2. Materials & Devices (MnD)
3. Circuits & Architectures (CnA)
4. Advanced Packaging & Heterogeneous Integration (AP/HI)
5. Algorithms & Software (AnS)
6. Power and Control Electronics (PACE)
7. Metrology & Benchmarking (MnB)
8. Manufacturing Energy Efficiency and Sustainability (MEES)
9. *Microelectronics Education and Workforce Development (MEWD)*

EES2 WG Highlight Talks by Month—THANK YOU

Working Group	Materials and Devices	Circuits and Architectures	Het Intg Adv Pkg	Metrology & Benchmark	Power & Control	Software Algorithms	Mfg Energy Efficiency
Speaker (s)	John B, SLAC Steffen, CTI & J.P. Aligned Carbon	Azeez, Metis & Emre, Stonybrook	Na Li, Carbice & Moinuddin, ANL	Jim B, NIST	Paul S. Sandia	Brian H Micron	Prashant N ORNL
Working Group Highlight Month (s)	March June	April	May	August	July	July	June

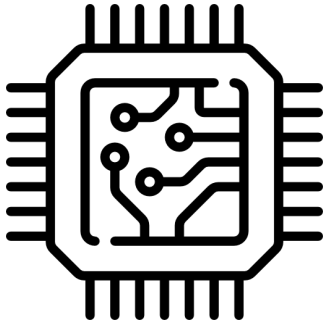
Microelectronics Education and Workforce, Tim W,



Northwestern

...but we've only just begun...

Materials & Devices WG/ Tech Boxes 1 of 2



Semi-conducting carbon nanotubes (CNTs): 5-10X

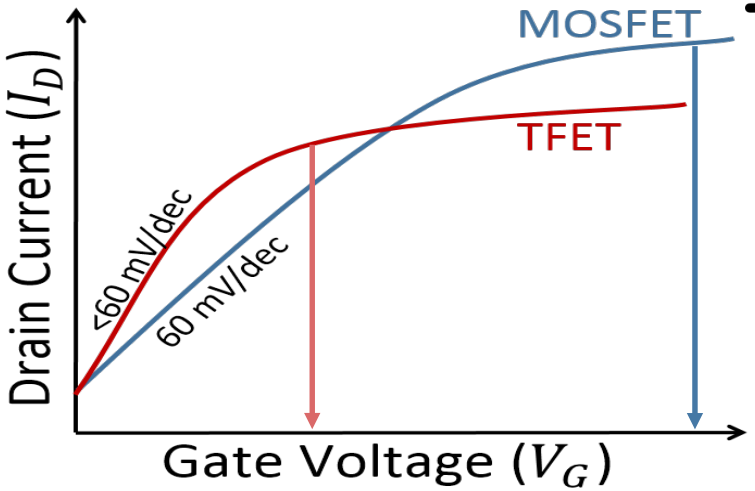
- In June, Steffen McKernan and J Provine, the CEO's, respectively of Carbon Technologies Inc. and AlighnedCarbon, showed results of CNT and CNT device manufacturing advances. As a result EES2 now projects that within 5 years CNTs could be commercially manufactured at purities and yields suitable for devices starting with RF, then sensors and then digital.

- Lab- scale CNTFETs have been shown to reduce switching power by at **least 7x** at an equivalent speed compared to Si CMOS. AMMTO intends to support additional RD&D to further scale up related CVD and atomic layer deposition (ALD) manufacturing processes

Materials & Devices WG/ Tech Boxes 2 of 2

Transistors: 10X(general) to 1000X (in specific applications)

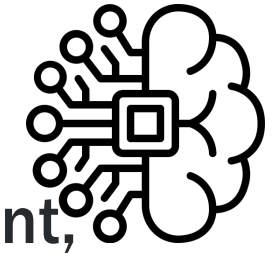
10X By Fall 2025, For AMMTO Lab Call, Sandia (PI Shashank Misra) will demo software and manufacturing for a **vertical TFET** for general purpose computing that is 10x more energy efficient than MOSFET



FeFET

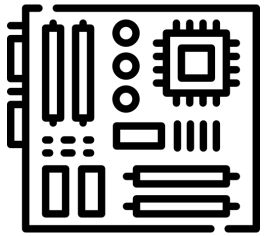
In March, John Baniecki of SLAC showed that a FeFET might be 1000X more energy efficient than MOSFET, but when included in a neural network architecture, was 10x more energy efficient. Need to understand what happens between Device & Software

Circuits and Architecture



- CIRCUIT 1000X: Emre in April showed that on chip local data movement, SRAM arithmetic is about 1000x more energy efficient than offchip DRAM.
- EDA: costs of just licensing EDA software have grown to tens of millions of dollars per project. But applications in EDA that now take thousands of human hours to complete could be sped up more than 1000x with an artificial intelligence (AI) program.
- ARCHITECTURE 1000X: Going from off chip digital to neuromorphic analog—such as with spiking neural networks, can cut energy use by 1,000x in Machine Learning (ML) applications. Azeez showed in April circuits that harvest the information token of data are on chip: electric charge when overwriting, moving or storing data and are Self limiting, self disabling & self regulating eliminate most of the inefficiencies (5X) seen with industry typical circuit architectures

Advanced Packaging & Heterogeneous Integration WG/Tech Box



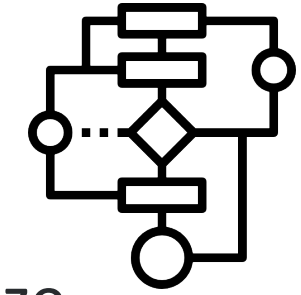
Advanced Packaging 3X-100X

- Advanced Packaging enables geometries that are nearly 20X more energy efficient than planar (2-dimensional) geometries.
- Na Li in May showed TSMC's 3D interconnect density (3DID) scaling out to 2040 at double efficiency every 2 years (to 100x)

Heterogeneous Integration: 1000X

- Moinuddin showed co-packaged optics (i.e., optical interconnects) may provide up to 10x additional improvement in efficiency and Na Li showed 3D hybrid bonding can increase interconnect energy efficiency by 3x.
- More Today from Volker!!

Algorithms and Software WG/Tech Box



1000X Our software group presented on past efforts to speed up algorithms, where a human software expert took 6 months to optimize software that would have otherwise taken a year to run, to run overnight. (400X efficiency increase) EES2 concludes that 1000x improvement in software energy efficiency will not require major breakthroughs—just the will, the expertise of key people and dedicated effort to do it.

50% LLNL HPC guys showed an algorithm method to put energy use caps on parts of the supercomputer that were not being used—even in peak use situations that could cut supercomputer energy **use in half overnight**.

Analysis Group / Tech Box

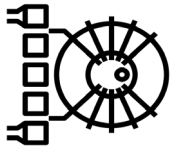
Analysis Team needs LOGO!

QUANTUM/NATURE-INSPIRED 1,000,000X OPPORTUNITY: Sadas' analysis comparing the energy used by the fundamental chemistry in the brain during a neural synapse versus the energy used by modern semiconductor chips shows that comparing the energy required to simulate chemistry (formation energy of benzene) in a digital computer is over a 1,000,000X than a quantum emulation of the same chemistry, which itself uses several orders of magnitude than the chemistry.

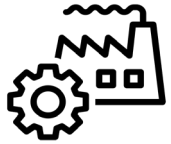
OVERALL OPPORTUNITY—1,000,000,000,000,000,000,000,000X Sadas' "Bits to Bitcoin" metric chart showing the energy used at various levels of computing shows that the energy difference between switching a Bit in a computer to mining a Bitcoin spans more than 24 orders of magnitude.

Crosscutting WG/Tech Box

Power and Control Electronics



Manufacturing Energy Efficiency and Sustainability

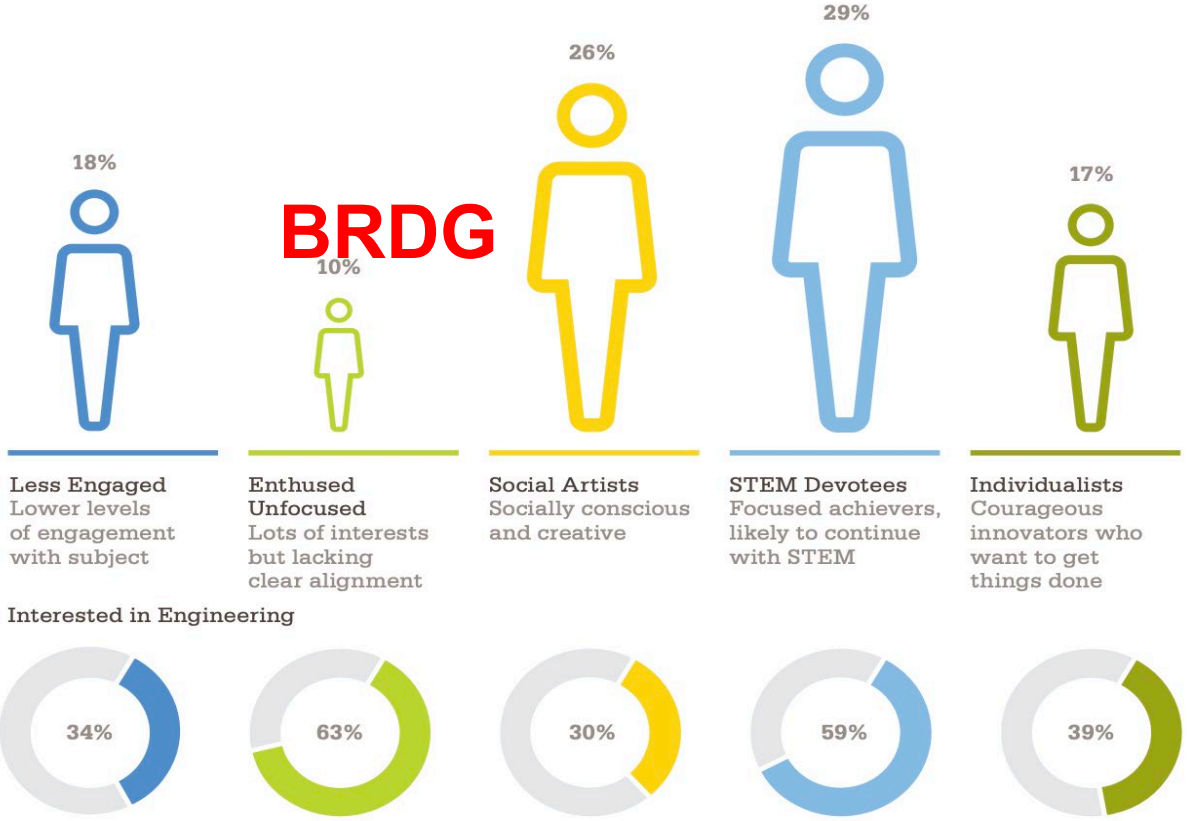


Metrology and Benchmarking

Cross Cutting WG are not expected to contribute directly to 1000X Energy Savings, but we are working on stories and factoids about why they are important—and like MEWD, they can have OWN GOALS

Education and Workforce Development Box

- Tim Wei estimated that US "traditional" STEM people supply will decline by as much as 50% by 2045 (e.g. need to at least double supply)



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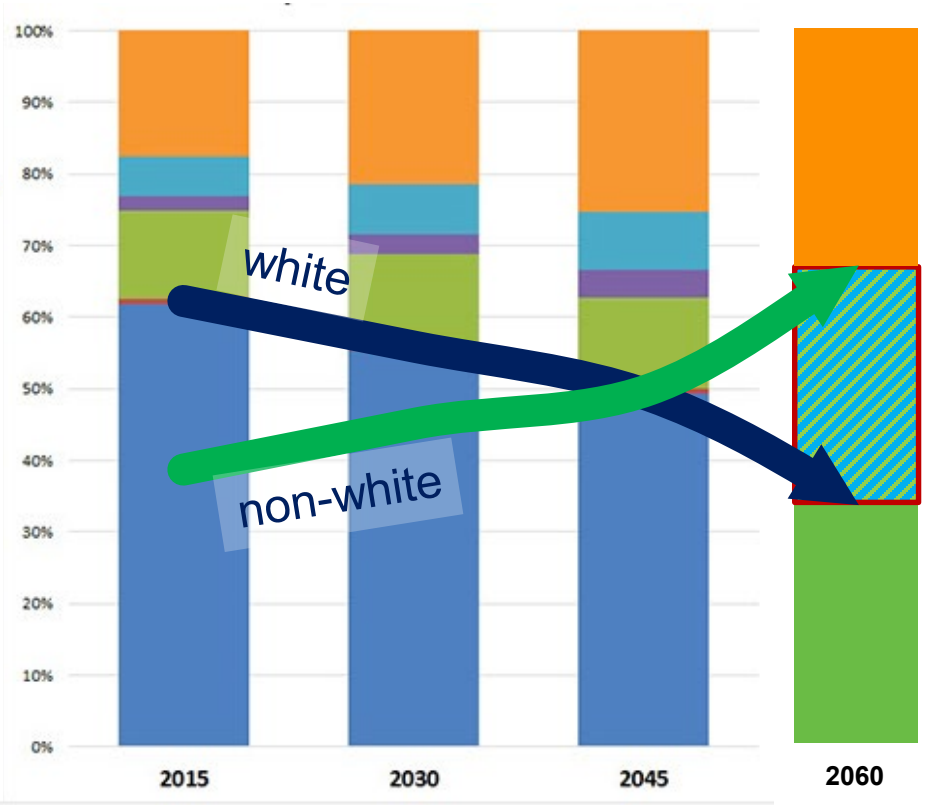

We can DO This!

- By Friday August 18—WG co-chairs:
  - Comment on Box or MAPT
  - Provide Head Shots!
- By Friday August 25—WG co-chairs:
  - Provide their and Pledgers Availabilities for October meeting.
- By Monday August 28—EES2 Secretariat
  - Sends Save the Date for Oct Meeting
  - Set WG Chapter writing deadline
  - Set other important deadlines involving important people

Thank you!

Q&A and Discussion