U.S. DEPARTMENT OF ENERGY

Office of ENERGY EFFICIENCY & RENEWABLE ENERGY

ADVANCED MATERIALS & MANUFACTURING TECHNOLOGIES OFFICE

EES2 ENERGY EFFICIENCY SCALING

1st Virtual Presentation

Day 1 Closing EES2 Workshop #7

Tina Kaarsberg, PhD
EES2 Workshop Co-Chair

June 21, 2023

https://microelectronics.slac.stanford.edu/amo-microelectronics

No New Pledgers Since May—has it become outdated???

EES2 ENERGY EFFICIENCY SCALING

We the undersigned agree to cooperate

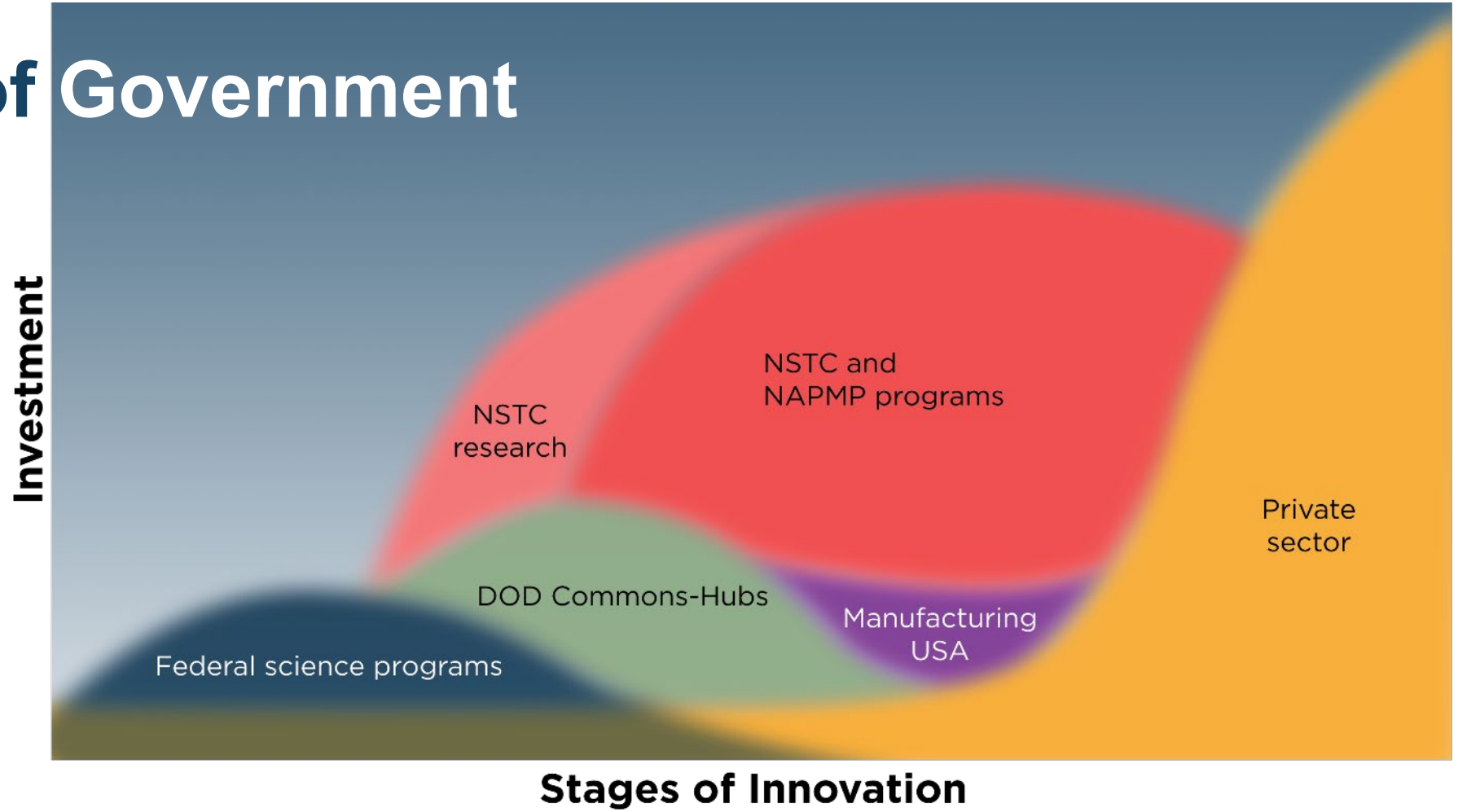
- To document and learn from the extraordinary record of microelectronics', including power electronics', energy efficiency such as increases greater than 1,000,000x in energy efficiency since the invention of the transistor nearly 75 years ago;
- To document and learn from microelectronics' past and forecasted future ability to enable all sectors of the economy to become more energy efficient and sustainable;
- To identify and publicize problems solved and opportunities offered by microelectronics' Energy Efficiency Scaling over 2 Decades (EES2);
- To publicize and identify sources to fund Version 1.0 (2022-2023) of the EES2 RD&D roadmap;
- To participate in Version 2.0 (2024-2025) of the AMMTO-led EES2 RD&D roadmap
- To explore formation of a partnership, perhaps "EES2 Allies" that enable the EES2 1000X efficiency goal by leading EES2 R&D Roadmapping after 2025 and by catalyzing the deployment of cost-effective technologies, including power electronics, needed to stay on the EES2 path of doubling microelectronics' energy efficiency every two years.

We do this because

- Microelectronics' life-cycle energy use is rapidly becoming unsustainable as microelectronics demand begins to outpace continuing efficiency improvements due to burgeoning computing, communication, and electrification demands
- EES2 is a key organizing principle that aims to help meet new energy demands
- The EES2 is a technology leadership path that provides economic and other public benefits.

Version 1.0 of the EES2 Roadmap is **near its end** I suggest we Replace **"participate in the AMMTO-led EES2 2022-2023 R&D Roadmap"** with text in Red

Whole of Government



Opportunity: CHIPS Publications lack Tech Specifics

- For example: May 10 DOC NIST: Vision and Strategy for the National Semiconductor Technology Center. The three GOALS (with our suggested specifics!) are

  - Extend U.S. leadership in foundational technologies (Energy Efficiency is a Key Leadership Path)

  - Reduce significantly the time and cost to prototype innovative ideas for member organizations (innovative efficiency ideas)

  - Build and sustain a semiconductor workforce development ecosystem (recruit from non-traditional “tribes” by focusing of environmental, social issues).

Funding Opportunities?

- EES2 Secretariat Can identify “Other Opportunities” schedule
- EES2 RD&D Roadmap Working Group Expertise needed for Keyword search!!

Department of Defense (DOD) Commons RFS (Hubs etc)

Defense Advanced Research (DARPA), Next-Generation Microelectronics Manufacturing (NGMM), and Electronics Resurgence Initiative (ERI) 2.0.

National Science Foundation (NSF)

(build on past energy efficiency work, current workforce),

Department of Commerce (DOC) NIST

NOFOs

NSTC

NAPMP (Adv. Packaging)

MfgUSA Consortia

Department of State Int’l CHIPS funding

June 6, 2023 CHIPS Industrial Advisory Committee Meeting

https://www.nist.gov/chips/industrial-advisory-committee

EES2 Relevant Excerpts from 3rd Meeting: June 6, 2023

https://www.nist.gov/system/files/documents/2023/06/07/4.%20Sequencing%20of%20Priorities.pdf

Why Use Case Studies? CHIPS IAC Public-Private Partnership's Sequencing Working Group says

Good way to identify specific needs across different contexts

What others are saying about 1000X Energy Efficiency Improvement

The IAC's PPP working group chose two topics of EES2 interest for its first Case Studies to scope possible activities that might be carried out at proposed NSTC :

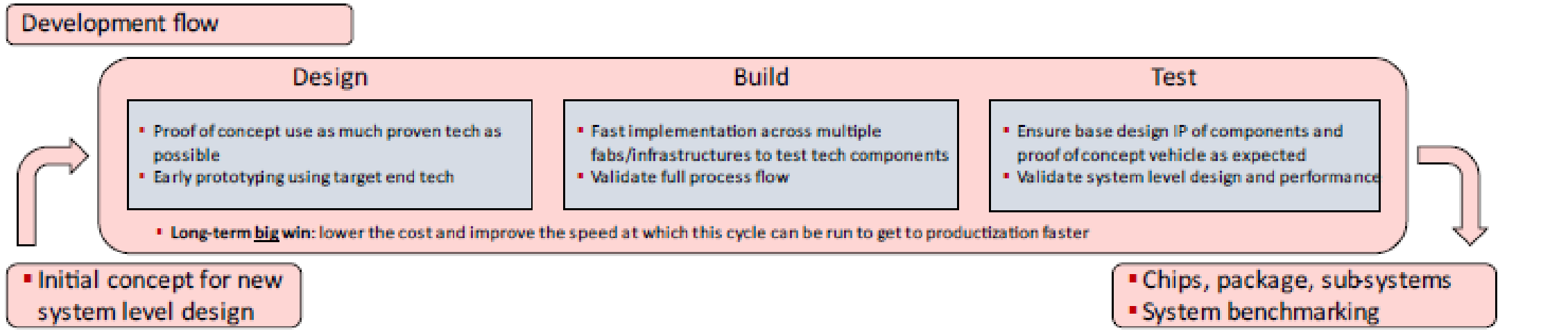
- A 100x energy efficiency boost for AI workload compute

Also

- Beyond 1-nm memory and logic (a startup company)

100X Energy Efficiency Boost

Through advances in logic, memory, heterogeneous integration



100x power reduction Grand Challenge

Design

Key issues:
- Lack of infrastructure to facilitate system level design across multiple parties
- Difficult to get early uses of new technology

- Common EDA platform
- Collaboration with workforce development for early users of the technology
- Seamless system-level design across multiple fabs

Prototyping

Key issues:
- Access to low volume logic and memory prototyping with some modifications
- Access to heterogeneous integration capability

- NSTC research topic for HI
- NSTC staff /researchers for prototyping
- Data protection
- NSTC central authority for project management

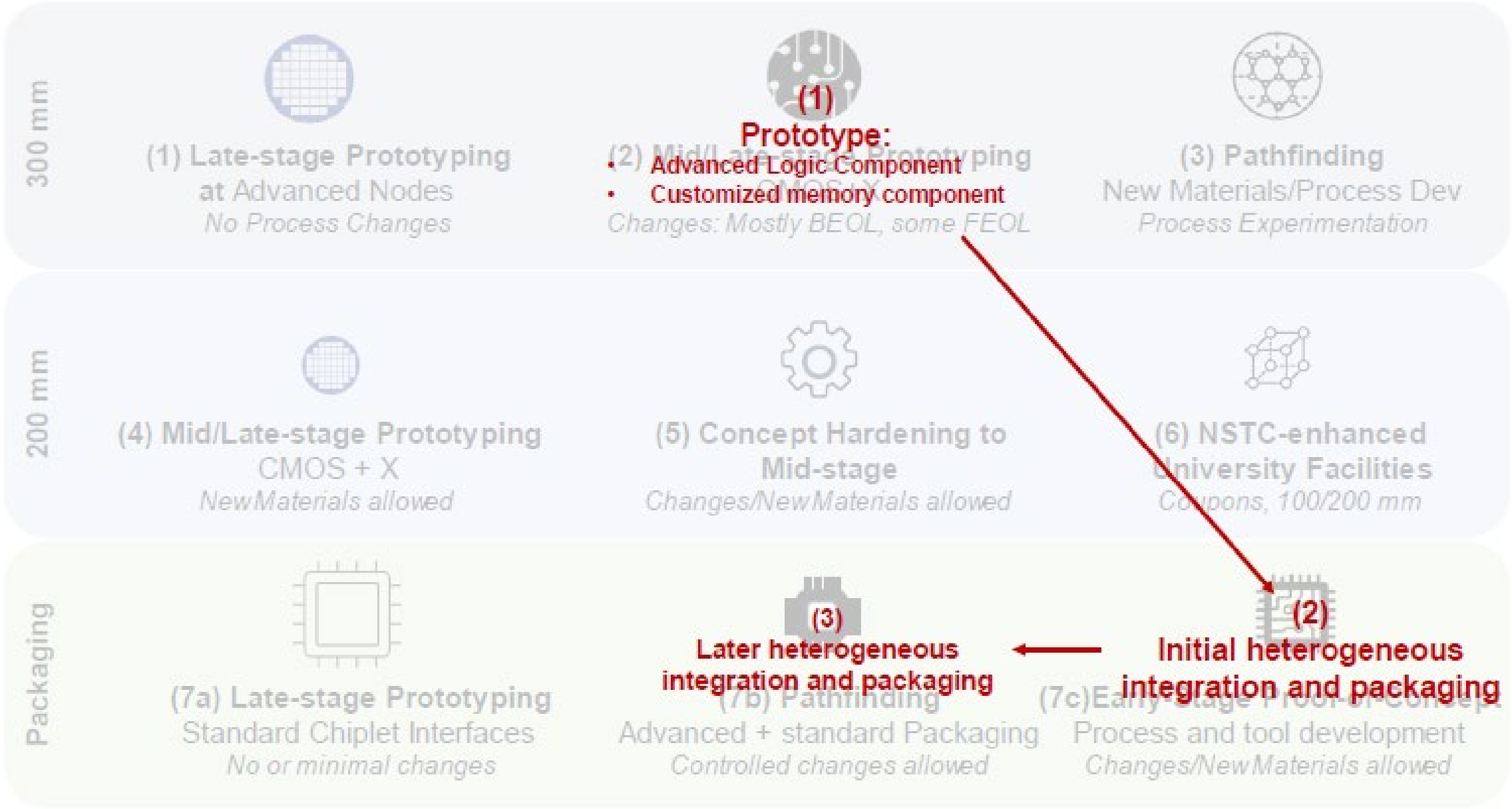
Benchmarking

Key issues:
- System level integration and testing
- Software ecosystem for new technology

- NSTC research topic
- NSTC staff computer scientists/researchers
- Collaboration with workforce development

- CHIPS funding to NIST allocated
- Needs NSTC decision and budget
- No obvious solution

Mapping: 100X Energy Efficiency Boost



What is Missing from These IAC Slides??

EES2 ENERGY EFFICIENCY SCALING

Stack

- Algorithms /Software
- Heterogenous Integration and Advanced Packaging
- Circuits and Architectures
- Materials and Devices

PLUS

- Metrology and Benchmarking
- Power and Control Electronics
- Manufacturing Energy Efficiency and Sustainability

Also what happens after end of CHIPS Funding (2023-2027)

Thank you!

Q&A and Discussion