U.S. DEPARTMENT OF ENERGY

Office of ENERGY EFFICIENCY & RENEWABLE ENERGY

Microelectronics' Energy Efficiency Scaling for 2 Decades (EES2) Closing and Next Steps

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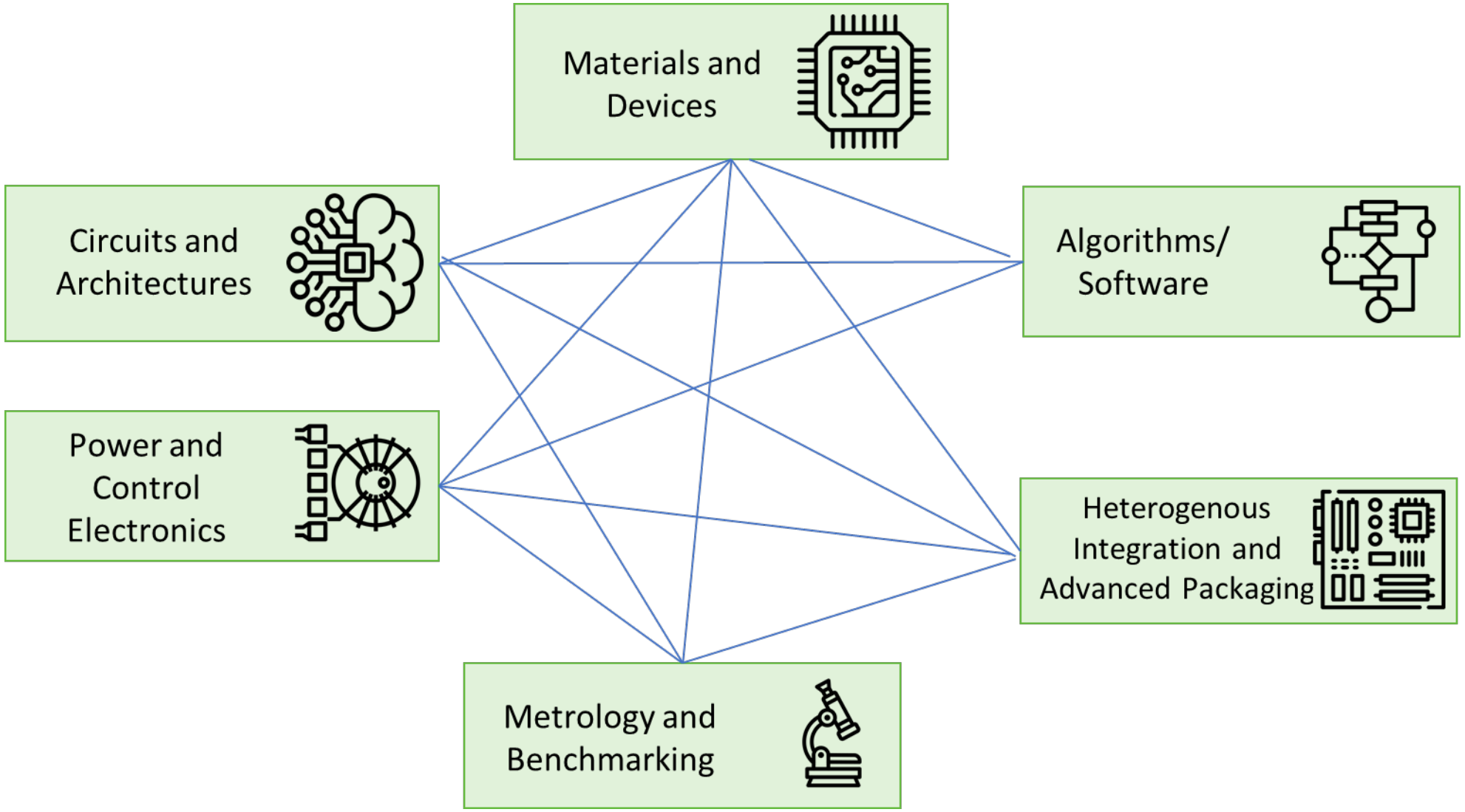
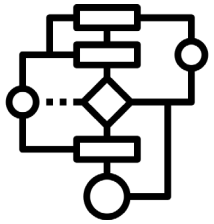
https://microelectronics.slac.stanford.edu/amo-microelectronics

Working Groups Inter-Relationships

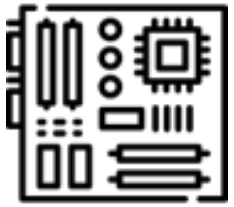


Key WG Role: Identify Biennial Contributions to Doubling

- Each contribution will vary in size, breadth timing (Examples below):

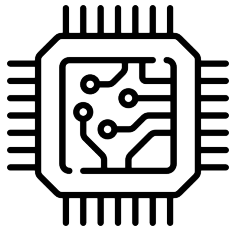


Energy-efficient algorithms and software may get some 10-100x+ wins in some applications in early years (~1-7 years)



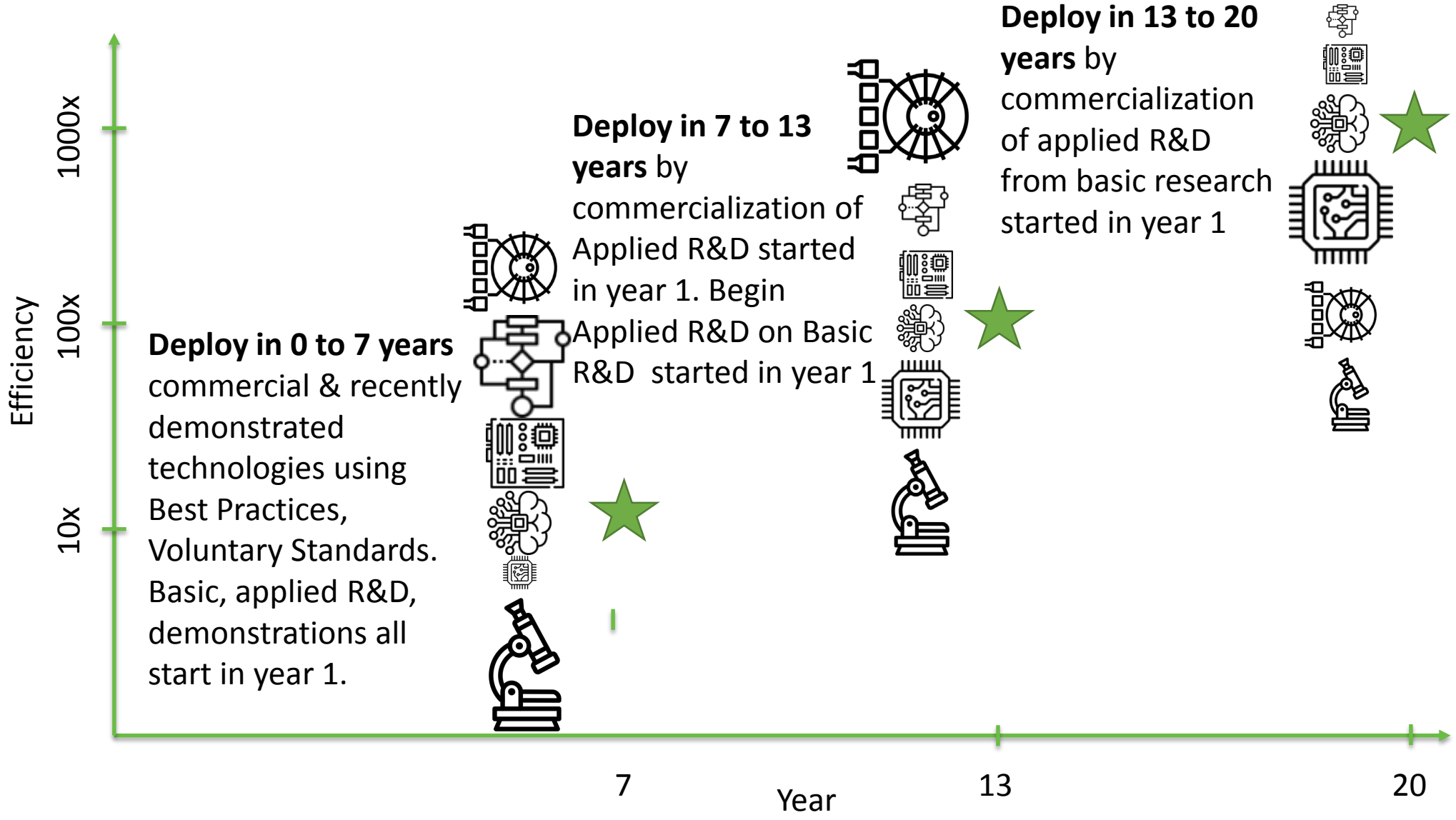
3D hybrid bonding can increase interconnect energy efficiency by 3x and interconnect density by 15x near term HI of ASIC chiplets for key apps in mid term ~1000X (~5-13 years)

Best practices in short term; Architectures like brain-inspired, compute in memory, etc., to reach 1000X+ for ML and other intensive apps midterm (~5-13 years)



New beyond-CMOS devices (e.g carbon electronics) with other device/interconnect/integration/packaging innovations w/architecture could contribute 1000X across the stack long term (~10+ years)

Tech Deployment Scenario for doubling every 2 years



EES2—not only a good idea, it's the…..Executive Order

- DOE Semiconductor Industry report in response to EO14017 "America's Supply Chains" picked up the EES2 goal and the need for a 20 year industry government partnership to implement it.
- White House crypto currency report in response to EO 14067 titled, "Ensuring Responsible Development of Digital Assets" and Executive Order 14008, "Tackling the Climate Crisis at Home and Abroad," recommends energy efficiency—including standards

CHIPS and Science Act was signed into law

- "CHIPS" appropriated $52B mainly at NIST (also DOD, State and NSF) (CHIPS already was authorized in FY20 NDAA). See https://www.nist.gov/chips

- Science part authorized $68B for DOE (also $81B at NSF). See https://science.house.gov/chipsandscienceact

- Science part included $1 Billion for Energy Micro Act. See SEC. 10731. MICROELECTRONICS RESEARCH FOR ENERGY INNOVATION "To provide for a comprehensive and integrative program to accelerate microelectronics research and development at the Department of Energy"

DOE held EES2 Implementation events

- **First EES2 open technical workshop (9/14/2022)**
  - 15 new ideas presented
  - All abstract submitters invited to pledge events

See: https://microelectronics.slac.stanford.edu/amo-microelectronics/presentations

- **First EES2 Pledge signing**
  - 20 signers including big and small industry, labs, NGOs
  - Initial proposal for EES2 Working Groups
  - Videos posted at
- **See:** https://microelectronics.slac.stanford.edu/september-20-2022-pledge

Other Key Inputs from Past Efforts

- NSF 2016-2022 –Energy Efficient Computing—from Devices to Architectures (NSF 16-526)
- DOE\BES Microelectronics BRN
- IEEE's Int'l Roadmap for Devices and Systems
- 2021-2022 AMO Semiconductor R&D for Energy Efficiency Workshop Series
- Interagency CHIPS Microelectronics R&D Strategic Plan
- *Your Input Here*

Other Key Inputs from ongoing and new efforts

- **NIST MAPT Technical Working Groups (TWG) A, B, C, D, E and F**
  - **See https://www.src.org/calendar/**
- **Nano4Earth**
  - **See https://www.whitehouse.gov/ostp/news-updates/2022/10/07/white-house-office-of-science-and-technology-policy-marks-national-nanotechnology-day-2022/ also https://www.nano.gov/nano4earthsignup**
- **Brain Science for Electronics (nsf.gov)**
- ***Your Input Here***

Next Steps: Expanded Pledge as our Guide

We the undersigned agree to cooperate

- To document and learn from the extraordinary record of microelectronics', including power electronics', energy efficiency such as increases greater than 1,000,000x in energy efficiency since the invention of the transistor nearly 75 years ago;
- To document and learn from microelectronics' past and forecasted future ability to enable all sectors of the economy to become more energy efficient and sustainable;
- To identify and publicize problems solved and opportunities offered by microelectronics' Energy Efficiency Scaling over 2 Decades (EES2);
- To participate in the AMMTO-led EES2 2022-2023 R&D roadmapping effort; and
- To explore formation of a partnership, an "EES2 Alliance" that enables the EES2 1000X efficiency increase goal by leading EES2 R&D Roadmapping after 2023 and by catalyzing the deployment of cost-effective technologies, including power electronics, needed to stay on the EES2 path of doubling microelectronics' energy efficiency every two years.

We do this because

- Microelectronics' life-cycle energy use is rapidly becoming unsustainable as microelectronics demand begins to outpace continuing efficiency improvements due to burgeoning computing, communication, and electrification demands
- EES2 is a key organizing principle that aims to help meet new energy demands
- The EES2 is a technology leadership path that provides economic and other public benefits.

We can DO This!

- We did it before for 30 generations
- The first pledgers' response has been amazing and humbling
- In the short- and medium-term
  - The best technologies are already on EES2 path*.
  - We understand the difference between the best and the rest*.
- For the long term –getting from 100X to 1000x and beyond
  - Shankar's analyses (2021 & 2022) show potential for 1,000,000X.
  - Consistent with SRC analysis.

Thank you

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