U.S. DEPARTMENT OF ENERGY

Office of ENERGY EFFICIENCY & RENEWABLE ENERGY

Closing Remarks for AMO Energy Efficiency Scaling (EES2) Goal Technical Workshop: Next Steps and Call To Action!!

Tina Kaarsberg, PhD

Advanced Manufacturing Office (AMO)

Next Steps: EES2 Pledges Guides both WG and signers

We the undersigned agree to cooperate

- To identify and publicize problems solved and the opportunities offered by microelectronics' Energy Efficiency Scaling over the next 2 Decades (EES2),
- To participate in the AMO-led EES2 2022-2023 R&D Roadmapping effort, and
- To explore formation of a partnership a "EES2 Alliance" that enables the EES2 1000X efficiency increase goal by leading EES2 RDD&D Roadmapping after 2023 and by catalyzing the deployment of cost-effective technologies needed to stay on the EES2 path of doubling microelectronics' energy efficiency every two years.

We do this because

- Microelectronics' life-cycle energy use is rapidly becoming unsustainable.
- EES2 is a key organizing principle that also counters this energy use.
- The EES2 is a technology leadership path that provides economic and other public benefits.

This Photo by Unknown Author is licensed under CC BY-NC

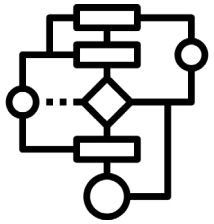
EES2 Working Groups must first Identify Most Urgent Problems

For example, EES2 Goal Technology Solutions must address:

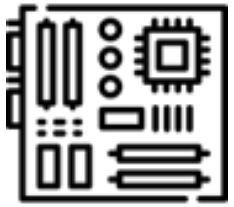
- **Energy efficiency increases from miniaturization are slowing down**
  - Time between successive technology nodes are extending
  - Miniaturization doesn't reduce energy use (as much) due to 'leakage'
  - Sub 10nm node chips' severe thermal management issues.
- **Energy demand of microelectronics is accelerating most in key areas**
  - Cryptocurrency now doubles energy use every 2 years.
  - Certain ML programs double energy use every 2-3 months.
  - Non-computing communications applications now > computing.
  - Electrification for decarbonization will further increase demand.

Key WG Role: Identify Biennial Contributions to Doubling

- Each contribution will vary in size, breadth timing (Examples below):

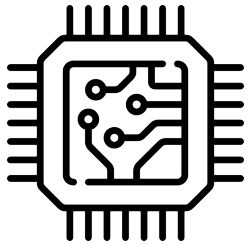


Energy-efficient algorithms and software may get some 10-100x+ wins in some applications in early years (~1-7 years)



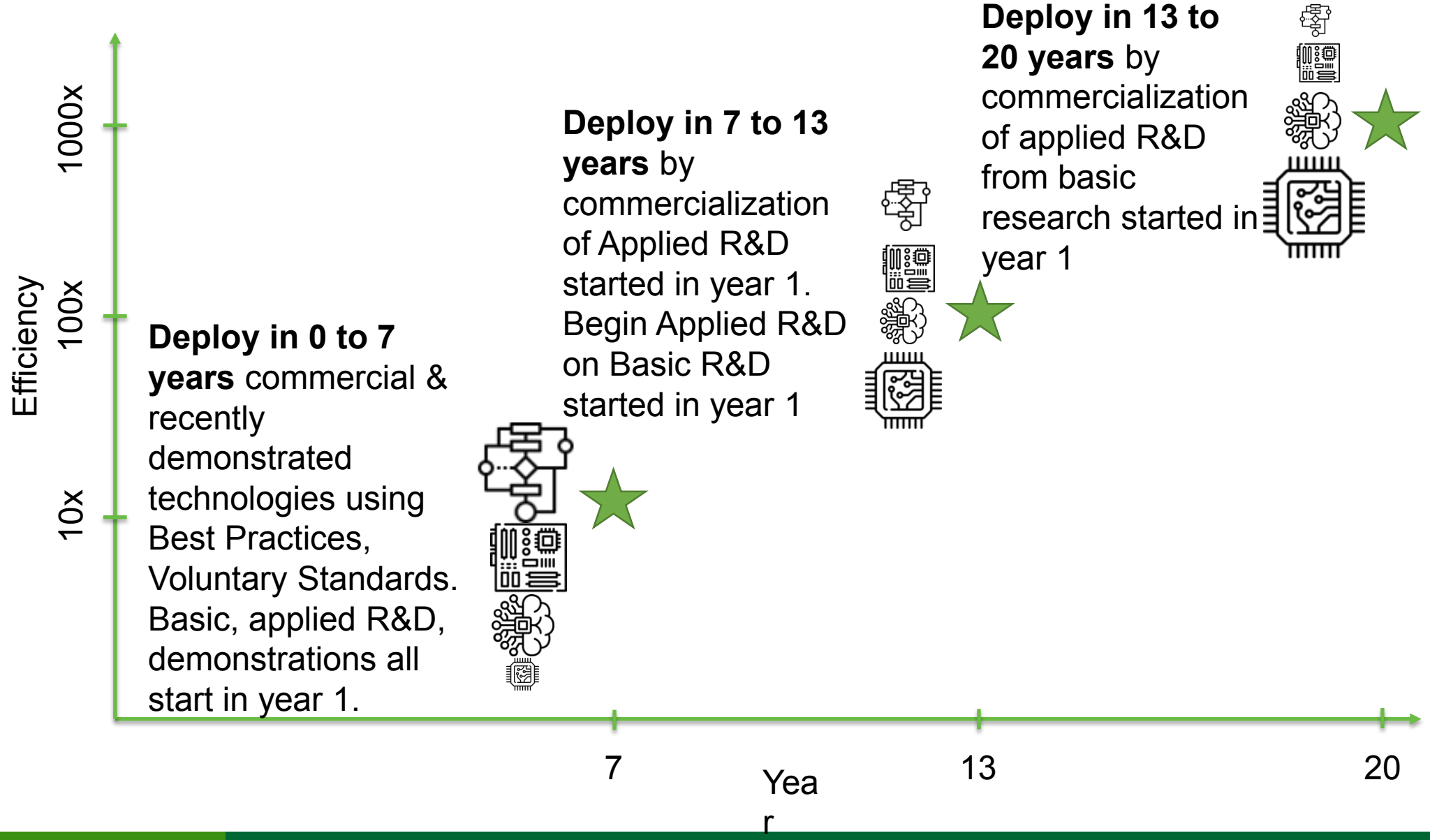
3D hybrid bonding can increase interconnect energy efficiency by 3x and interconnect density by 15x near term HI of ASIC chiplets for key apps in mid term ~1000X (~5-13 years)

Best practices in short term; Architectures like brain-inspired, compute in memory, etc., to reach 1000X+ for ML and other intensive apps midterm (~5-13 years)



New beyond-CMOS devices (e.g. carbon electronics) with other device/interconnect/integration/packaging innovations w/architecture could contribute 1000X across the stack long term (~10+ years)

Tech Deployment Scenario for doubling every 2 years



EES2 Goal Cooperation Pledgers

U.S. DEPARTMENT OF ENERGY

NSF

AMD

arm

Micron

SYNOPSYS®

cadence®

Microsoft

CARBON TECHNOLOGY INC

NANTERO

LIQID

SRC Semiconductor Research Corporation

AMERICA'S FRONTIER FUND

Sandia National Laboratories

Argonne NATIONAL LABORATORY

BERKELEY LAB

NREL NATIONAL RENEWABLE ENERGY LABORATORY

SLAC

We the undersigned agree to cooperate

- To identify and publicize problems solved and the opportunities offered by microelectronics' Energy Efficiency Scaling over the next 2 Decades (EES2),
- To participate in the AMO-led EES2 2022-2023 R&D Roadmapping effort, and
- To explore formation of a partnership a "EES2 Alliance" that enables the EES2 1000X efficiency increase goal by leading EES2 RDD&D Roadmapping after 2023 and by catalyzing the deployment of cost-effective technologies needed to stay on the EES2 path of doubling microelectronics' energy efficiency every two years.

We do this because

- Microelectronics' life-cycle energy use is rapidly becoming unsustainable.
- EES2 is a key organizing principle that also counters this energy use.
- The EES2 is a technology leadership path that provides economic and other public benefits.