U.S. DEPARTMENT OF ENERGY

Office of ENERGY EFFICIENCY & RENEWABLE ENERGY

Welcome to Energy Efficiency Scaling (EES2) Goal Technical Workshop

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https://microelectronics.slac.stanford.edu/amo-microelectronics

AMO Semiconductor R&D for Energy Efficiency Series

Workshop 1: Integrated Sensor Systems
January 25-26, 2021

Workshop 2: Ultra-Precise Control for Ultra-Efficient Devices
April 21-23, 2021

Workshop 3: Mfg. and Integration Challenges for Analog and Neuromorphic Computing
August 11-13, 2021

Workshop 4: Advanced Packaging for 3D Micro-electronics
January 12-13 /19-20, 2022

KEY TAKEAWAYs

- SRC forecast of unsustainable semiconductor energy use: 25% of planetary energy by 2030
- Data deluge from increased deployment of sensor systems requires minimizing the amount of data created and communicated from the sensor node
- Ultra-energy-efficient (>10X) semiconductor devices to counter trends require ultra-precise manufacturing processes
- Increased industry-government partnerships and access to state-of-the-art facilities for academic and small business researchers to prototype new devices and circuit designs is needed

Co-led by DOC National Institute of Standards and Technology (NIST)

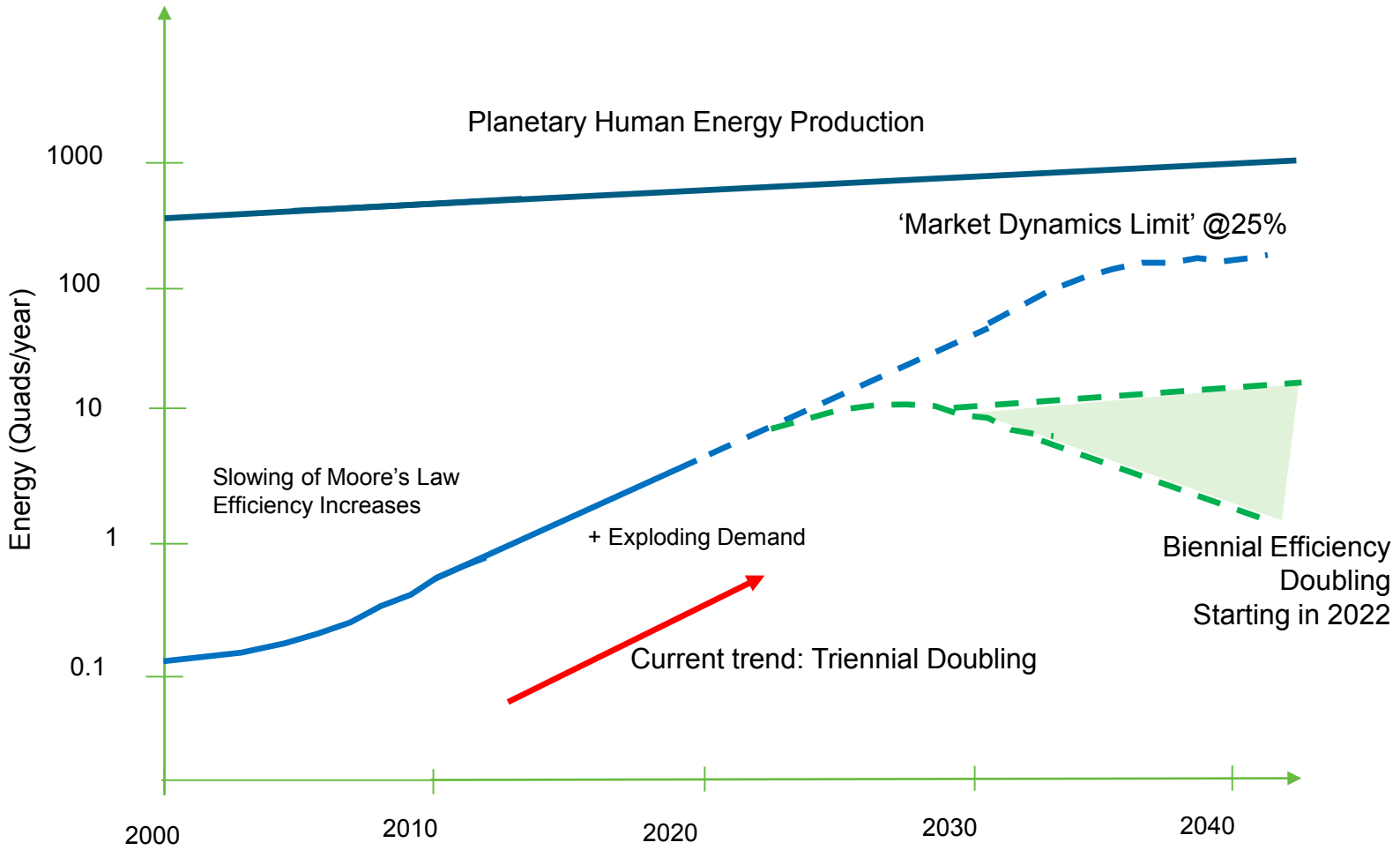
- Analog and neuromorphic computing approaches and devices can enable efficiency and speed improvements in areas of sensing, communication, and machine learning by >1,000X and potentially 1,000,000 with bio-inspired design
- Advanced packaging is a key first step in integrating advanced technologies in memory, compute, and neuromorphic devices, while improving energy efficiency

Co-sponsored by DOE Office of Science and Semiconductor Research Corporation

- Co-packaged optics (i.e., optical interconnects) may provide up to 10x improvement in efficiency
- 3D hybrid bonding can increase interconnect energy efficiency by 3x and interconnect density by 15x
- **1000X EES2 Goal Announced**

Co-led with DOC NIST

Background: *Semiconductor Research Corporation Projections vs EES2*



NOTE: log scale on vertical axis

- Era of doubling energy efficiency biennially through planar geometric scaling ended around 2010.
- New application spaces – whose energy use is accelerating (especially AI) are driving increased energy use since 2010. After 2020, electrification adds another fast-doubling driver.
- Depending on demand and implementation, EES2 will flatten or possibly even reduce semiconductor energy use

Source: Based on SRC Decadal Report (2021)

Energy Efficiency Scaling Goal (EES2) and Implementation

EES2 Goal: a new scaling "law" – "energy efficiency scaling" (EES2) – to help organize research, development, demonstration, and deployment (RDD&D) to specifically

DOUBLE microelectronics' energy efficiency every TWO years to reach 1000X energy efficiency

EES2 Implementation Events

- **TODAY!**: Technical Presentations on technologies that could contribute to the biennial doubling and 1000X efficiency goals: public event featuring Dr. Sadasivan Shankar (SLAC) and Dr. David Patterson (Google) and many more.
- 9/20/2022: EES2 Pledge Signing and R&D Working Group kickoff with Department of Energy Undersecretary Richmond and Leadership from industry, non-profits, academia and other government partners.

GOAL: Why we need Efficiency Scaling and Why we can do it

We need it because

1) Computing energy use (doubling every 3 years - 10X in a decade) could cause economic meltdown and undermine efforts to reduce climate change.
2) Other microelectronics energy use (e.g., communication, electrification for decarbonization) also have short doubling times.

We can do it because

- In the short- and medium-term
  - The best technologies are already on EES2 path*.
  - We understand the difference between the best and the rest*.
  - We've collected examples across the stack of 10-1000X efficiency improvements (*to be presented **today**).
- For the long term --getting from 100X to 1000x and beyond
  - Shankar's analyses (2021) shows potential for 1,000,000X efficiency improvement.
  - Consistent with SRC analysis. **UPDATES TODAY**

Working Group Categories TBD, Schedule is outlined

EES2 R&D RoadMap (Version 1) to be issued Fall 2023