Infineon Vertical and Substrate Power Delivery Concepts:

Enabling Energy Efficiency of Computing Semiconductors

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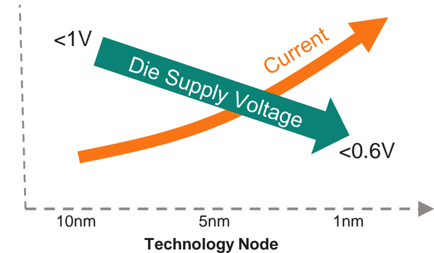
High Performance System On Chip Power Trends

Higher SoC Currents

- Advanced nodes move to lower voltages
  - P=IV, thus supply currents increase
- Increasing processor core count and chiplet integration further increase currents
  - Enabled by improved thermal management techniques
- System I^2R losses reduce overall computing “Energy Efficiency of computing Semiconductors” (EES)



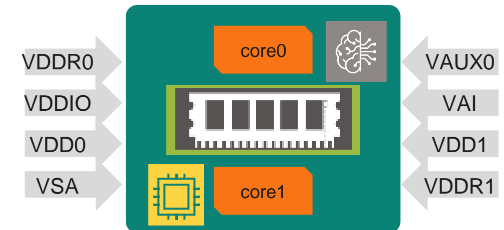
Higher currents vs. shrinking technology nodes

More Rails

- Driven by increased chiplet integration with different voltage requirements
- Break up of large high current voltage planes to improve voltage regulation accuracy
- Granular power domains needed for full compute efficiency optimizations

Higher Density

- EES will drive more efficient compute SoCs leading to more cores and processors
- Power will most likely remain constant: Extends Moore’s law in benchmarked systems
- More rails drive density since physical environments are generally not changing
- Power density needs to follow…



More rails with more chiplets

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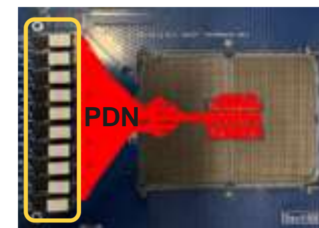
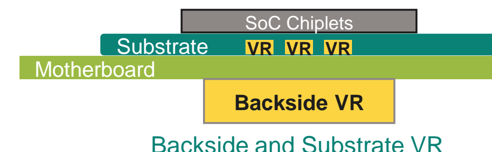
Maximize Efficiency: Power Delivery Change is Needed

- Traditional Power Deliver Networks (PDN) are mostly lateral
  - Single sided motherboard assembly with easy access to cooling
  - 200 µOhm PDN: only 12.5W loss at 250A, but 200W at 1000A (I^2=1E6)
  - We see SoC roadmaps to 2300A (I^2=5.3E6)
- PDN limits transients
  - Adding more capacitors helps address but slows VR bandwidths

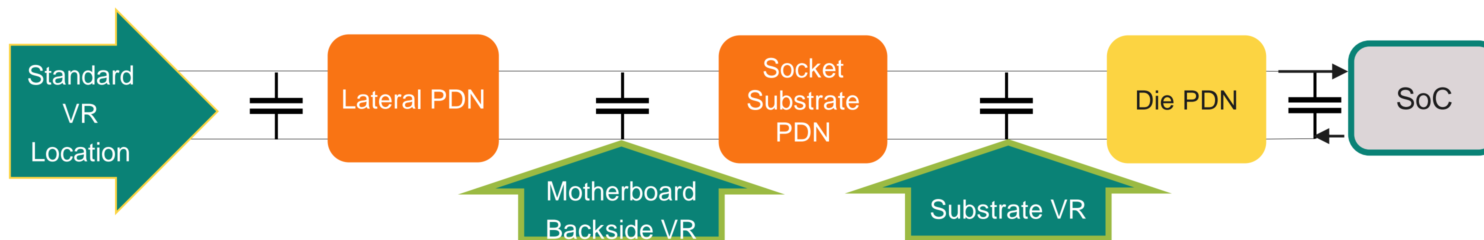
- **Vertical power delivery is needed**
  - A combination of both Backside and Substrate VRs enables EES challenges



Lateral Power Delivery Network (PDN) with a standard VR location



Backside and Substrate VR



- Addresses majority of PDN loss if supplied by higher voltages (48V)
- Transient impedance is reduced but still limited
- Moderate area, height and thermal constraints. New infrastructure.

- Optimal transient location, and also addresses nearly all of PDN loss if supplied by higher voltages (12V)
- Severe area, height and thermal constraints. Higher risk.

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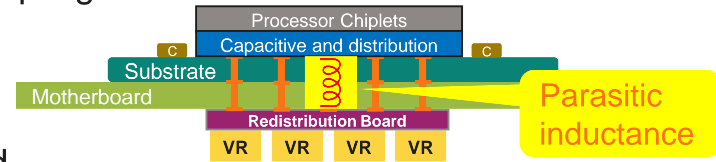
Increase Capacitance in SoC to Increase Efficiency

Problem: Back side modules interfere with traditional passive decoupling capacitor locations

Impractical Solution: 50MHz+ VR bandwidths are needed to manage voltage excursions if backside bulk capacitance is removed

- Bad for efficiency due to high voltage transition losses
- Lowering VR supply voltage as a band-aid improves VR efficiency at the cost of increased PDN losses



Backside with minimal lateral interconnect and remote decoupling capacitors

Root Cause Proposal: Capacitive decoupling closer to the SoC die

- Ideal transient benefit while enabling lower VR switching frequencies
  - 5-10MHz VR switching frequencies might be a good compromise of density and efficiency
  - Remote caps help increase VR bandwidths to enable faster di/dt in parasitic inductors (V=Ldi/dt)
- Higher voltage supplies (12V target) to the processor address PDN
- Potential areas of capacitance integration:
  - On die trench caps
  - Wafer on Wafer (WoW) capacitive stacking
  - Substrate capacitance (top, embedded or land-side)

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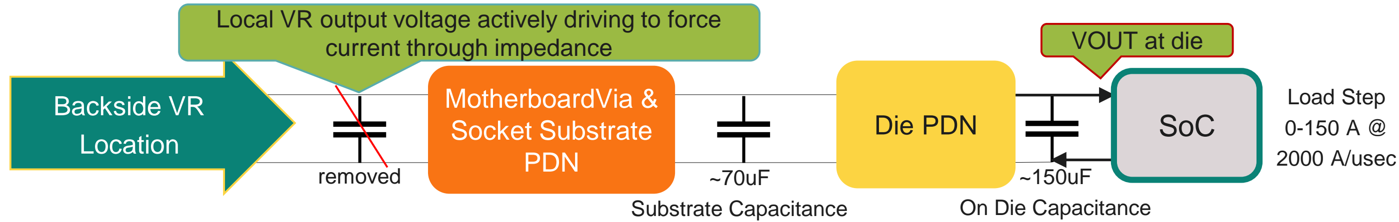
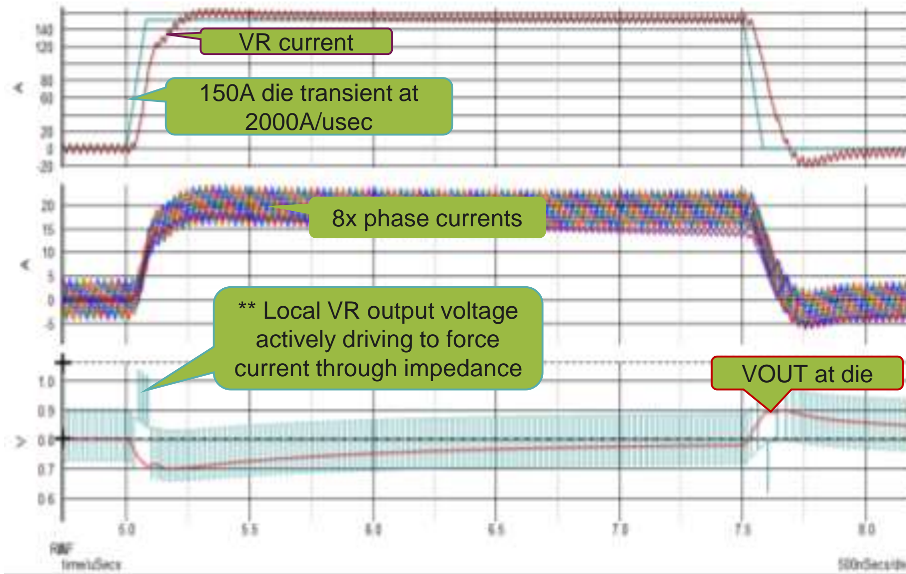
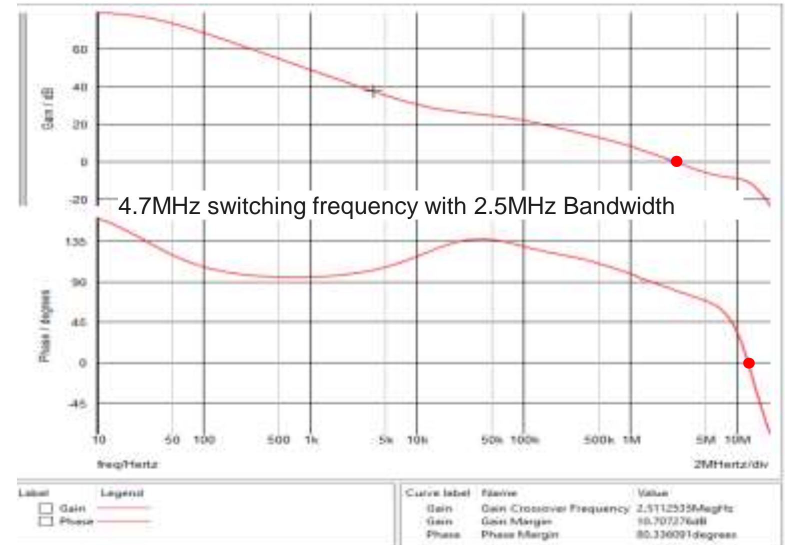
5MHz Switching with 2.5MHz Bandwidth
5V VIN to 0.8V VOUT with no local VR output caps







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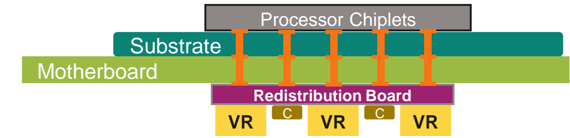
Backside Vertical Power Modules

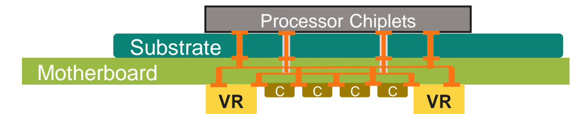
- Modules enable density, shorter PDN
- Thermal management requires physical environment unchanged

Three placement configurations considered:

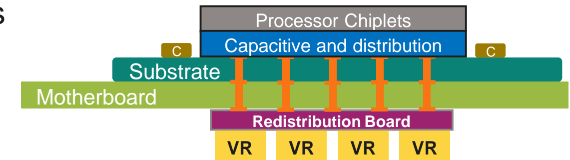
1. **Directly under the SoC** with VOUT to VIN BGA alignment through motherboard vias.
   - Requires a redistribution board which introduces lateral losses
   - Decoupling capacitors transition onto the redistribution board
2. **Peripheral to decoupling capacitor banks**
   - Similar lateral losses but maintains decoupling for lower risk
3. **BVM with remote decoupling capacitance**
   - SoC on-die and/or substrate and top-side capacitors to manage initial transients
   - No backside capacitors enable increased Voltage Regulator (VR) control loop bandwidth to drive motherboard output impedance
   - Increasing rail counts challenge module density



Backside with minimal lateral interconnect and local decoupling capacitors



Peripheral Backside with large local decoupling field and reduced lateral interconnect



Backside with minimal lateral interconnect and remote decoupling capacitors

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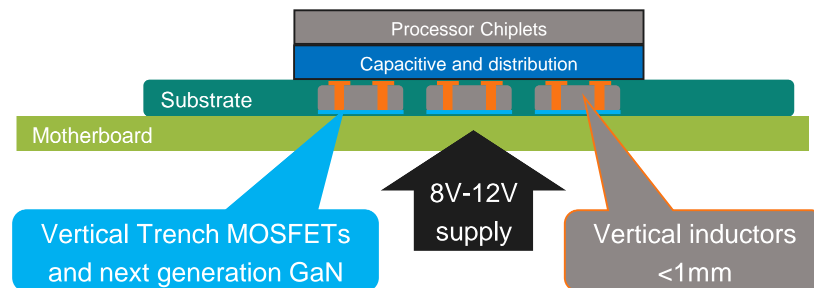
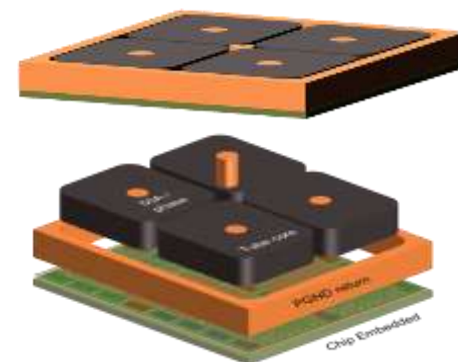
Substrate Voltage Regulators (SVR)

Benefits
- SVR increases system voltages, reduces PDN loss
- Enables localized granular power
  - SoC can act as the VR controller
- Faster transient response due to reduced output impedance
  - Removes motherboard and socket impedances from the output
  - Remote capacitors enable wide control loop bandwidth
  - VIN input impedance still needs to be considered for peak magnetizing currents



Risks
- SVR integration requires full SOC commitment
- Mitigation: establishing a common ecosystem
  - Common power conversion elements which can be integrated by the SoC developer
  - Standards needed
- Infineon is working on several concepts to enable standardization



5-10MHz Substrate Voltage regulator Module (SVM) Concept

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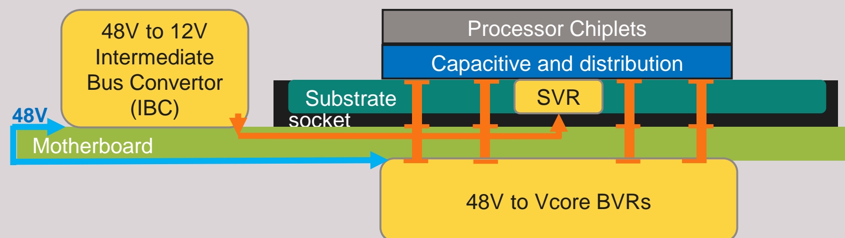
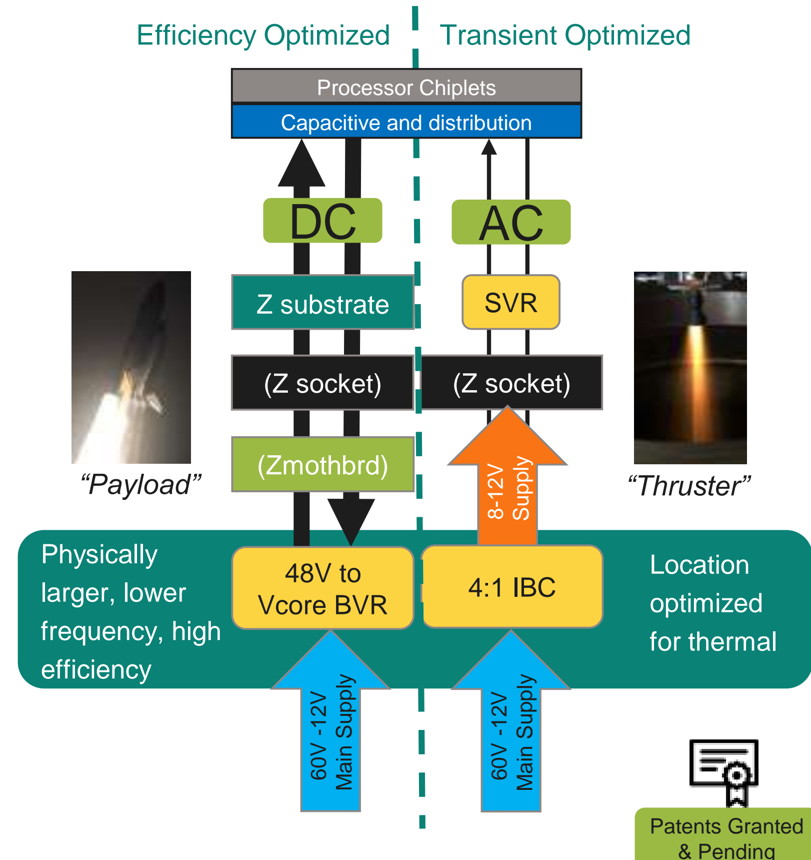
Hybrid Control Concept: Optimized Power Delivery based on VR location

Motivation
– Address proximity limited power delivery through hybrid power distribution

- Infineon has established control algorithms which allow multiple voltage regulators to regulate a common voltage
- VRs with lower AC impedance can switch at higher frequencies, optimized for transient response ("*Thruster*")
- Larger VRs with access to cooling can switch at lower frequencies optimized for high current delivery ("*Payload*")





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Call-to-action: Opportunities for Standards & Technology Investment

Standardization and investments will establish common ecosystems, accelerate higher efficiencies, and establish roadmaps for continued improvement.

1. **SoC Decoupling Capacitance:** Fund studies on how best to scale onboard SoC capacitance / mm^2
   - Potential capacitance concepts: wafer-on-wafer, silicon substrate and substrate embedded capacitance
   - Establish high frequency VR requirements to drive a common ecosystem

2. **Backside Vertical Power Delivery**: Establish scalable backside power module physical standards
   - Top and bottom cooling infrastructure and “Z” dimensions to enable an ecosystem
     - Target applications: Server, AI accelerator, PCIE standards supporting Backside VPD

3. **Substrate Vertical Power Delivery**: Fund technology developments and prototypes towards achievable standards
   - Reduce integration risk through a common ecosystem and technology
   - Develop necessary passive, silicon and package technologies
   - Define technology roadmap requirements for continued efficiency and density advancements

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Key Takeaways:

1. **Power delivery infrastructure needs to change**, allowing backside vertical power delivery with sufficient cooling in order to minimize Power Delivery Networks (PDN) losses, maximize efficiency
   – Standardization would enable fastest path to higher efficiency
2. **Capacitance needs to get closer to the SoC**, allow for lower frequency and higher input supply voltage converters to meet transients while reducing PDN losses and maximizing system efficiency
3. **Substrate Power Conversion will be a necessity** as core voltages continue to reduce while currents and rail counts continue to increase
4. **Hybrid Power Delivery** is needed to optimize transient response and power delivery thermal management and density

- **Infineon** establishes control algorithms allowing multiple voltage regulators to regulate a common voltage
- We develop 48V to Vcore, 48V intermediate buss topologies, and substrate VR concepts
- Infineon also invests in high frequency OptiMOS™, CoolGaN™ and packaging to enable future Energy Efficiency Semiconductors
  – Please contact Danny.Clavette@Infineon.com for your high performance SoC power delivery requirements

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