DoD Microelectronics Commons

A National Network for Defense Microelectronics Innovation

Energy Efficiency Scaling over 2 decades, (EES2) Workshop

February 16, 2023

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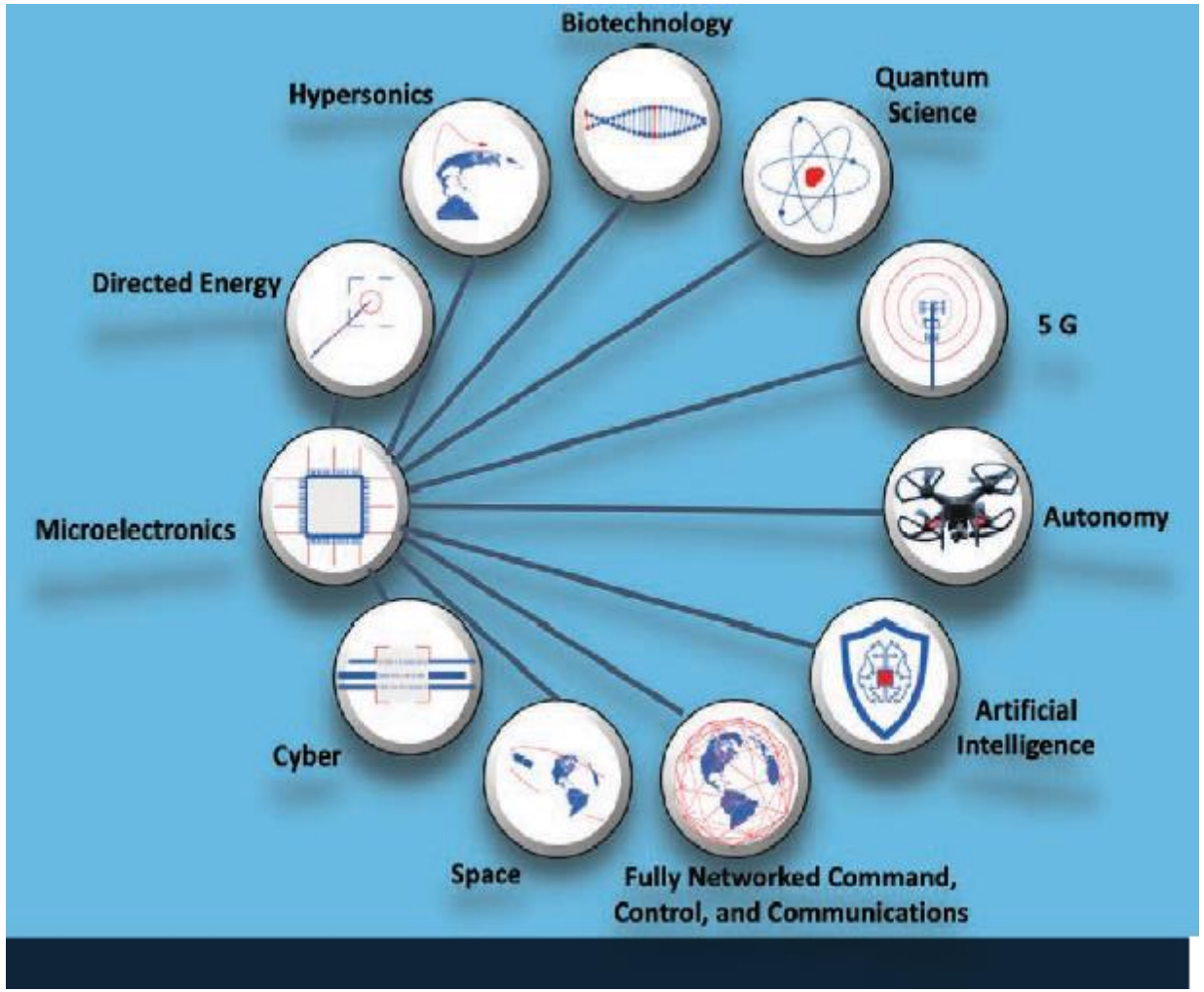
OUSD (R&E) Microelectronics Modernization

HTTPS://WWW.CTO.MIL @DODCTO @OUSDRE

If there is any inconsistency between the material presented here and the Request for Solutions (RFS), **the RFS shall take precedence**.

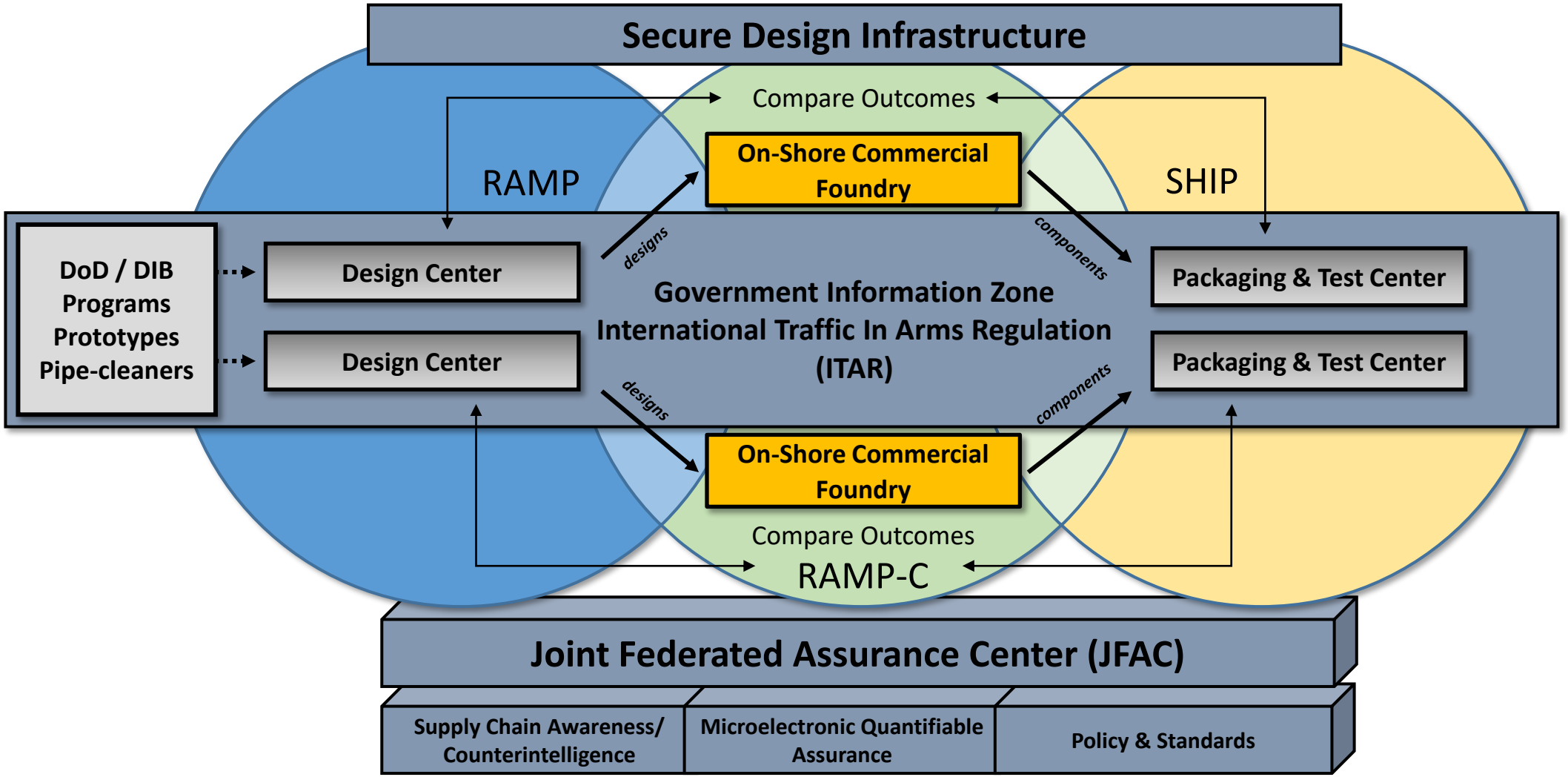
The Microelectronics Commons RFS will be posted on *www.sam.gov* and *https://nstxl.org/opportunity/microelectronics-me-commons/*

CRITICAL TECHNOLOGY SYNERGIES: MICROELECTRONICS



- Autonomous Drones
- AI Chips
- Self Driving Vehicles
- Energy Efficiency For Edge Computing
- Military Applications

T&AM Program Enabling Access to State of the Art (SOTA)



Access to State of the Art (SOTA) Roadmap: Microelectronics

Fiscal Years →	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032+
Foundry Access		**Access to SOTA US commercial foundries for DoD specific designs (Intel & Global Foundries)**									
		Fund 2-3 runs per year in commercial ≤ 22nm node technology for DoD specific designs				*Establish 2 runs per year in commercial ≤5nm node technology for DoD Specific Designs*					
RAMP		**Rapid Assured Microelectronics Prototypes (Microsoft Team, Qualcomm)**									
		Demonstration of secure design capability via 3 prototypes by the DIB in SOTA technology				*Cloud based commercially scalable, quantifiably assured, design and manufacturing flow capability fully utilized by DiB*					
RAMP-C		**RAMP-Commercial (Qualcomm, Intel)**									
		Intel 18A test chip designs completed		*Intel 18A PDK*		*High Volume (25k/wpms) leading edge (<5nm) foundry capability for QA dual-use COTS & custom DoD ICs*					
Emulation and EDA		**Emulation Pathfinder for QA Design Flow (AFRL)**									
		JSF F35 & PEO SUB prototype demonstrations of emulation based QA design flows				*Qualified emulation based QA design flow capability*					
SAHARA		**Structured Array Hardware for Automatically Realized Applications (Intel)**									
		Prototype Structured Array chip demonstrated (50M gates)				*Fully developed SAHARA capability to efficiently convert existing FPGA designs to Structured ASIC, at an onshore SOTA foundry with security*					
Design Acceleration and Transition		**New Starts in FY23 – Design Acceleration and Transition Efforts**									
		Contract awards(s) for new T&AM activities									

LEGEND

Enhanced Capabilities

Key Milestones | *Unfunded Option*

Major Investments to Mature the Domestic SOTA Microelectronics Ecosystem

Future SOTA Microelectronics Needs

- Domestic access to mature SOTA materials, foundries, and packaging
- Ecosystem alignment to DIB and POR

NorthPole Neural Inference Processor

➢ Disruptive Innovation

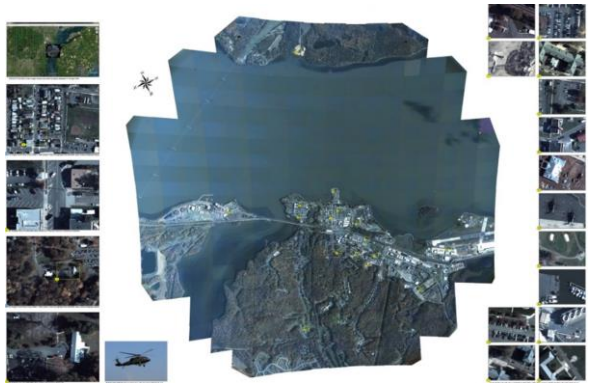
- **1st gen IBM TrueNorth was the most energy-efficient processor for deep inference**
  - 50X more energy-efficient than lowest-power GPU
- **2nd gen IBM NorthPole leaps beyond TrueNorth**
  - 3,000X more computation
  - 640X larger neural networks (CNN, MLP, RNN)
  - Only 4X more transistors (22 billion)

➢ Broad Application Potential

- **Configurable clock rate and supply voltage**
  - 25MHz~400MHz, 0.67V~0.82V
- **Adaptive chip run power for broad use cases**
  - 5W~60W chip power
- **Breakthrough peak energy efficiency and low latency**
  - ResNet50, Yolov4 benchmarks

➢ DoD Mission Needs

- **Huge data volume and velocity**
  - 95% of data/intelligence lost without real-time on-board analytics
- **Approaches for Processing**
  - **NorthPole (GF 12nm):** 4 chips, 200W at 2/4/8-bit mixed precision
  - **GPU (V100 TSMC 12nm):** 20 chips, 5,000W



➢ DoD/DoE Common Interest

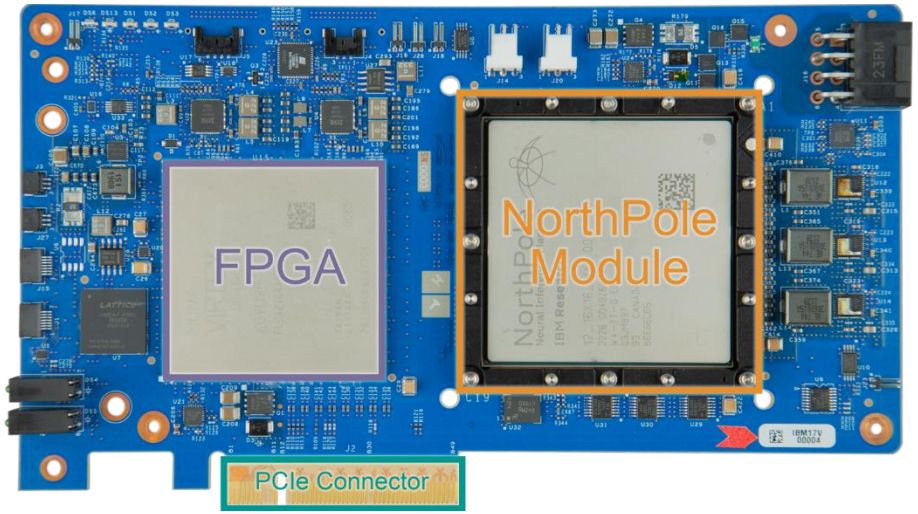
- **Exascale AI Inference in low-power, low-volume form factor with applications to intelligence, mobile data centers, and supercomputing.**

➢ Extend, secure, and protect US advantages in AI, Autonomy, etc.

- **NorthPole surpasses other AI inference chips on energy efficiency, space efficiency, and latency**
- **Export controlled HW&SW** – subject to EAR
- **Government-Purpose Rights** – IPs for future development
- **US based design & manufacturing** – Global Foundries 12nm

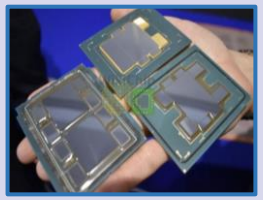
➢ Transition Pathways

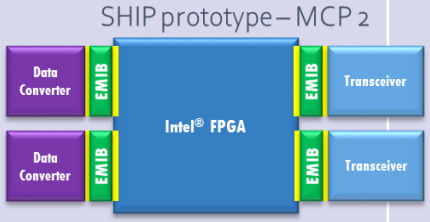
- **PCIe Form Factor Board**
- **Software Development Kit with Easy Migration**
- **Transition Workshop (1st Workshop planned for March 16, 2023, still possible to register and attend)**



Access to Advanced Packaging Roadmap: Microelectronics

Fiscal Years →	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032+
State-of-the-art (SOTA) Heterogeneous Integrated Packaging (SHIP) - Digital		**Digital Packaging and Test Capability**			**Digital Packaging Access Model Implementations**						
				Sustainable Access Model in Place			*Sustainable Access Model Stand Ups*				
					Advanced Digital Packaging Capability Development						
		Prototype Demonstrator Multi-Chip Packages					*Packaging Capability Development Projects*				
		Demonstrator Chiplet			**Advanced Digital Packaging Technology Maturation**						
							Technology Maturation & Prototyping Projects				
State-of-the-art (SOTA) Heterogeneous Integrated Packaging (SHIP) - RF		**RF Packaging and Test Capability**			**RF Packaging Access Model Implementations**						
							Sustainable Access Model Stand Ups				
		Packaging Technology Releases			**Advanced RF Packaging Capability Development**						
		Assembly Design Kits		*Factory Setup Complete*			*Packaging Capability Development Projects*				
		Prototype Demonstrator Multi-Chip Packages			**Advanced RF Packaging Technology Maturation**						
							Technology Maturation & Prototyping Projects				
STEAM PIPE **Strategic Transition of microElectronics to Accelerate Modernization by Prototyping and Innovating in the Packaging Ecosystem**		**Prototyping to Lower Risks for Transition**									
		Requests for Solutions									
							Estimated Prototype Deliveries				





LEGEND

Enhanced Capabilities

Key Milestones

Sustained access to domestic SOTA advanced packaging for DoD system modernization

Future Advanced Packaging Needs

- A self-sustaining model for DoD and the DIB to procure cutting edge microelectronics in a high mix – low volume environment.

Heterogeneous Integration (HI) and SWAP Benefits

Why HI?

- Modular approach vs. Monolithic approach
- Not every logic function (IP) needs to be designed in the same process node (HI)
- Leveraging IP in the form of chiplets
- Current industry trend has led to chiplets on silicon interposers
- Includes latest IC packaging 2.5D, 3D, FOWLP technologies
- Optimize nodes required for ideal performance and cost

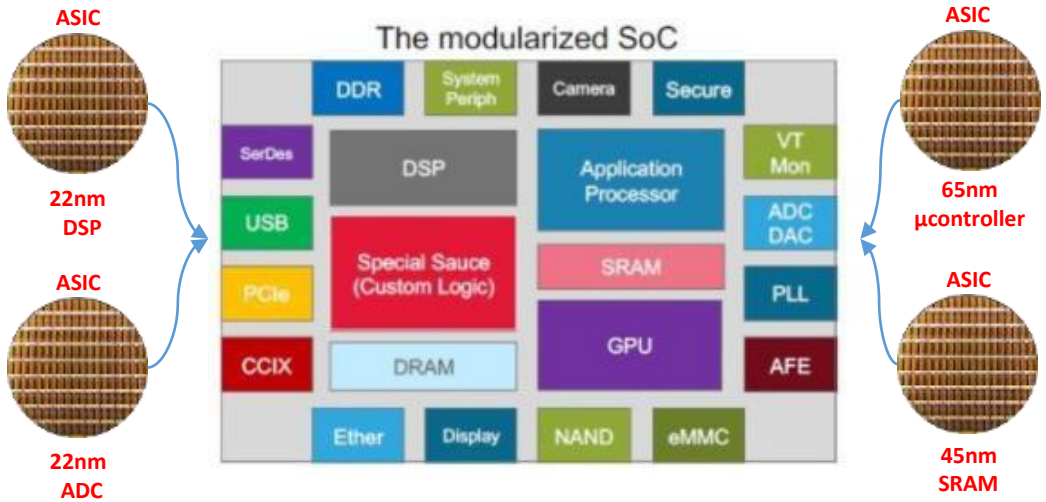
SHIP is leveraging commercial HI solutions to improve SWAP savings and system performance

Expected SWAP Savings:
8x relative to current solution

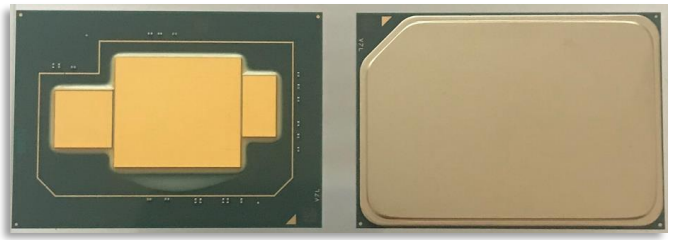
Through HI enabled SWAP savings, MCP-1 will deliver:

- ✓ Unprecedented spectral agility
- ✓ Enhanced signal processing
- ✓ Lower power consumption
- ✓ Improved thermal management

Notional HI MCP



SHIP-D functional parts have been delivered to lead DIB partner to prove SWAP benefits



MCP-1 consisting of two chiplets integrated with an FPGA

MCP-1 finished package

Lab-to-Fab Transition of Microelectronics Technologies

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Research Universities, **Start-ups** have facilities for Lab prototyping but face barriers to demonstrating manufacturability in a Fab.

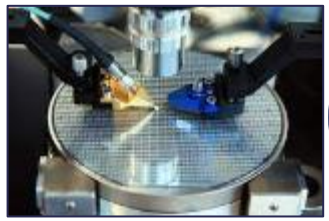
Core Facilities or Foundries/Fabs provide access to early stage Fab prototyping.

Microelectronics Commons aims to enable lab-to-fab prototyping– evolve microelectronics laboratory prototyping to foundry/fab prototyping – in domestic facilities.

The Microelectronics Commons: Innovation from Lab-to-Fab

Innovation Barriers

- Lack of access to existing fabs for lab-to-fab prototyping
- High capital costs for process and metrology tooling to support manufacturing of microelectronics technologies
- High Intellectual Property (IP) and Electronic Design Automation (EDA) design license costs
- Lack of domestic access to chip carriers, and packaging materials to support integration of electronics
- Lack of workforce talent and expertise to support technology transition



Partnerships

Technology Transition

Workforce Development

End State

- **Sustained partnerships** between emerging technology sources, manufacturing facilities, and interagency partners
- **Rapid transition** of early-stage microelectronics research to proven technology in domestic foundries
- Expand **domestic** microelectronics fabrication capability
- Enhance microelectronics **education** to bolster the microelectronics engineering workforce
- Develop a **pipeline of talent** to bolster local semiconductor economies and grow the domestic semiconductor workforce

Democratize access to capabilities needed for lab-to-fab prototyping

Microelectronics Commons Addresses the Valley of Death

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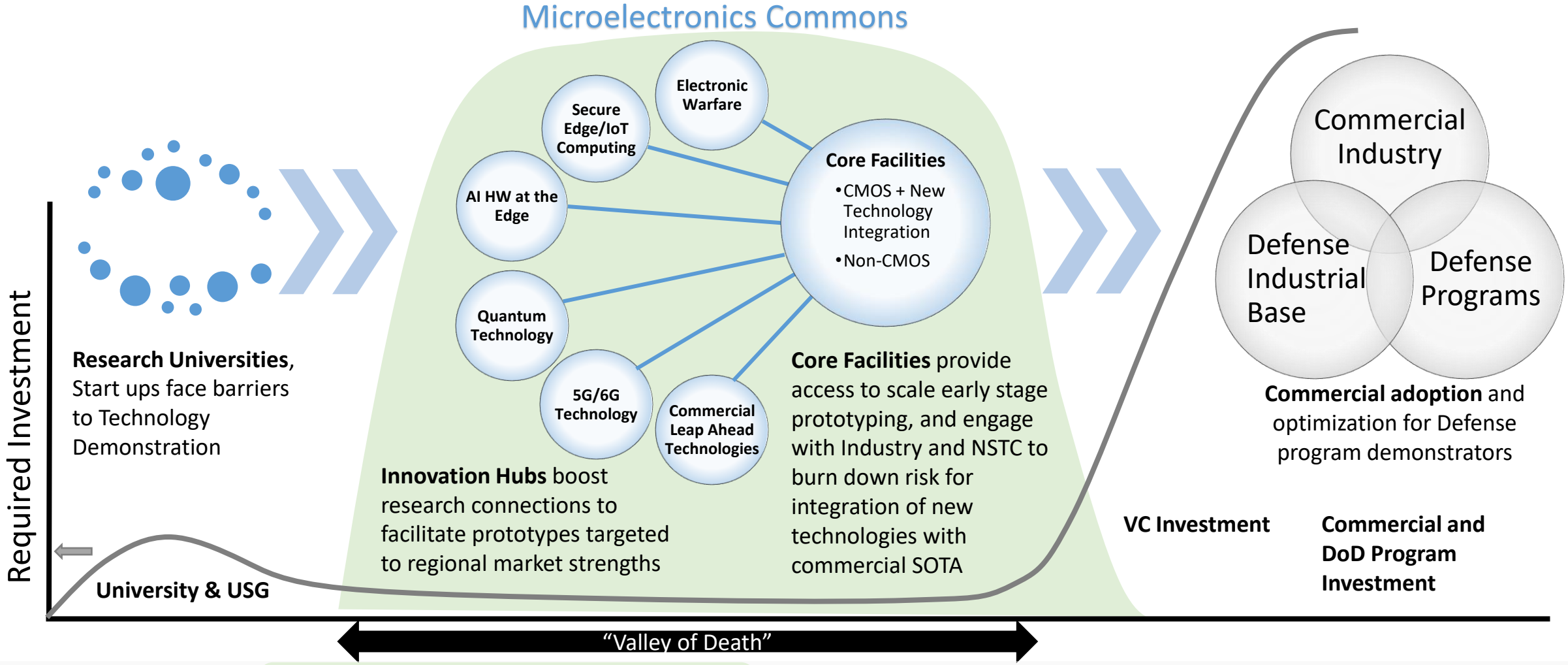


Accelerating Artificial Intelligence Hardware at the Edge

- Desired End State
  - A fab prototype for eventual deployment in AI-enabled systems for edge applications
    - Enables overmatch performance in operational situation awareness and decision making in a wide variety of DoD missions
    - Hubs and Cores need to facilitate the lab-to-fab prototyping and testing of these AI hardware platforms
- Technical Gaps
  - Need AI Computing systems that can do both training and inference at the edge
  - Throughput and energy efficiency of existing AI edge computing systems is hampered by the vast amount of multi-domain sensor and operational data; places constraints on size-weight-and-power (SWaP)
  - AI computing architectures and algorithms for real-time warfighter decision support in complex environments.
  - Realizing the potential of emerging neuromorphic computing chips and AI accelerators to address critical applications and high performance at scale

Progression from Concept to Product

S&T

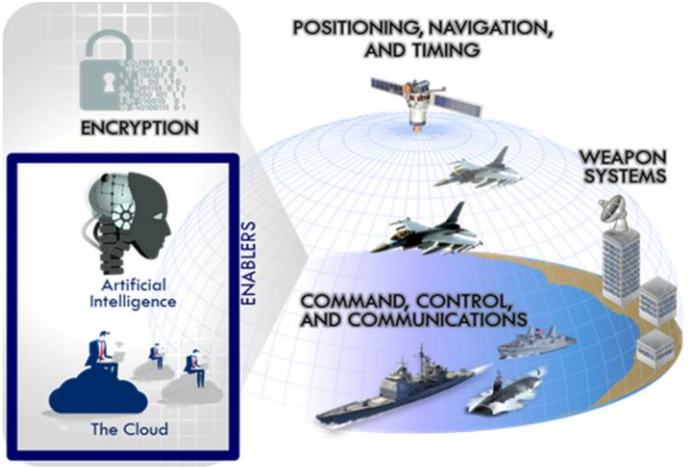
- Electronic Warfare
- Secure Edge/IoT Computing
- AI HW at the Edge
- Quantum Technology
- 5G/6G Technology
- Commercial Leap Ahead Technologies

Tech Demos

- RAMP
- RAMP-C
- SHIP
- T&AM Prototypes

Application Platforms

- Aircraft
- Submarines
- Ships
- Space Systems
- Ground Systems
- Missile Defense
- C4ISR



Lab-to-fab prototyping bridges valley of death from laboratory research to foundry/fab prototyping

Hubs and Cores

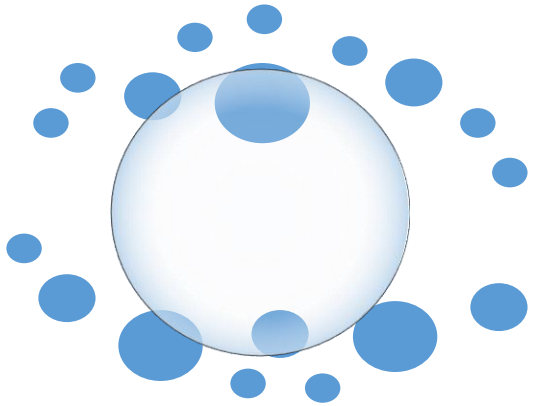
Hubs

A network of regional entities with lab prototyping capabilities and sources of microelectronics talent for onshore, lab-to-fab transition of semiconductor technologies while ensuring workforce training.

Hubs:

- Have the flexibility to bring in members from any region to be successful in their lab-to-fab efforts.
- Connect researchers and designers to prototyping capabilities targeted to strengths in the Hub's technical topic areas.
- Will be centers of expertise for one or more of the six critical technology areas.

Microelectronics Commons



Goal

To connect regional organizations through the Hub to accelerate lab-to-fab prototyping based on proximity and to strengthen local economies through a workforce that supports those regions.

Cores

Fabs/foundries that have scalable capacity beyond what the regional hubs can provide.

Cores serve to:

- Further complement and amplify the work of the regional hubs; for example, ≥200 mm wafer fab for Silicon CMOS-compatible technologies and ≥100 mm wafer fab for compound semiconductors.
- Engage with commercial fabs and align them better to commercial processes to facilitate transition to commercial and defense companies.
- Provide access to repeatable processes, back-end manufacturing/integration and full flow-fabrication.

Commons Will Support Infrastructure

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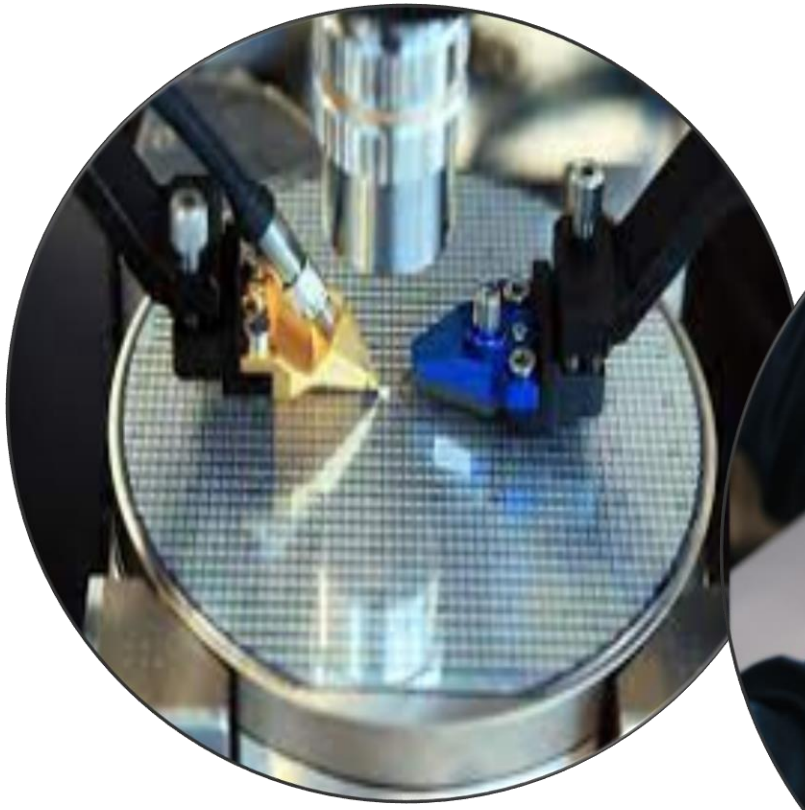
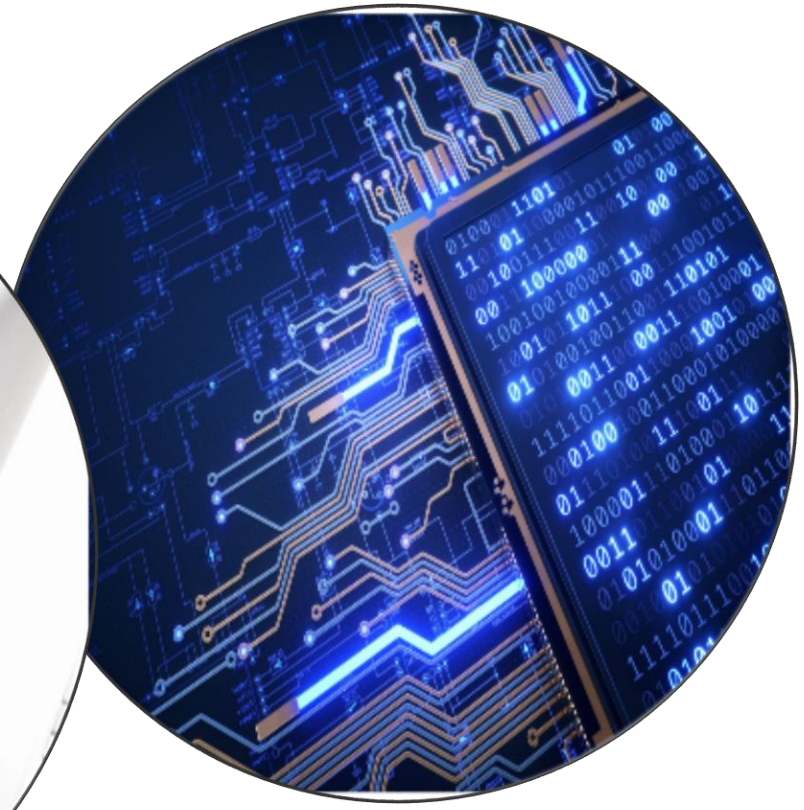
Human Infrastructure ....





Physical Infrastructure ....

Digital Infrastructure ...

Infrastructure is foundational to the success of the Microelectronics Commons

Role of Projects

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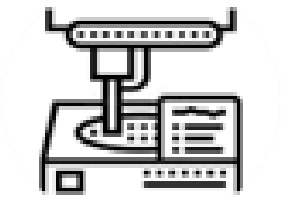
Support

Operational expenditures such as tooling maintenance and staff



Facilitate

Capacity increase of existing **infrastructure** through, for example, support for required staffing

Build

Additional infrastructure needed for successful prototyping as the Hubs mature

Develop

Talent and **technologies** in parallel

Challenge

Challenges incentivize the collaboration required for Cores to better align Hubs with commercial processes to **facilitate transition of technologies.**

This enables Hubs to better **support** the broader base of **researchers and designers.**

Projects enhance the value of infrastructure through staffing and utilization of lab and fab facilities

Hub Models

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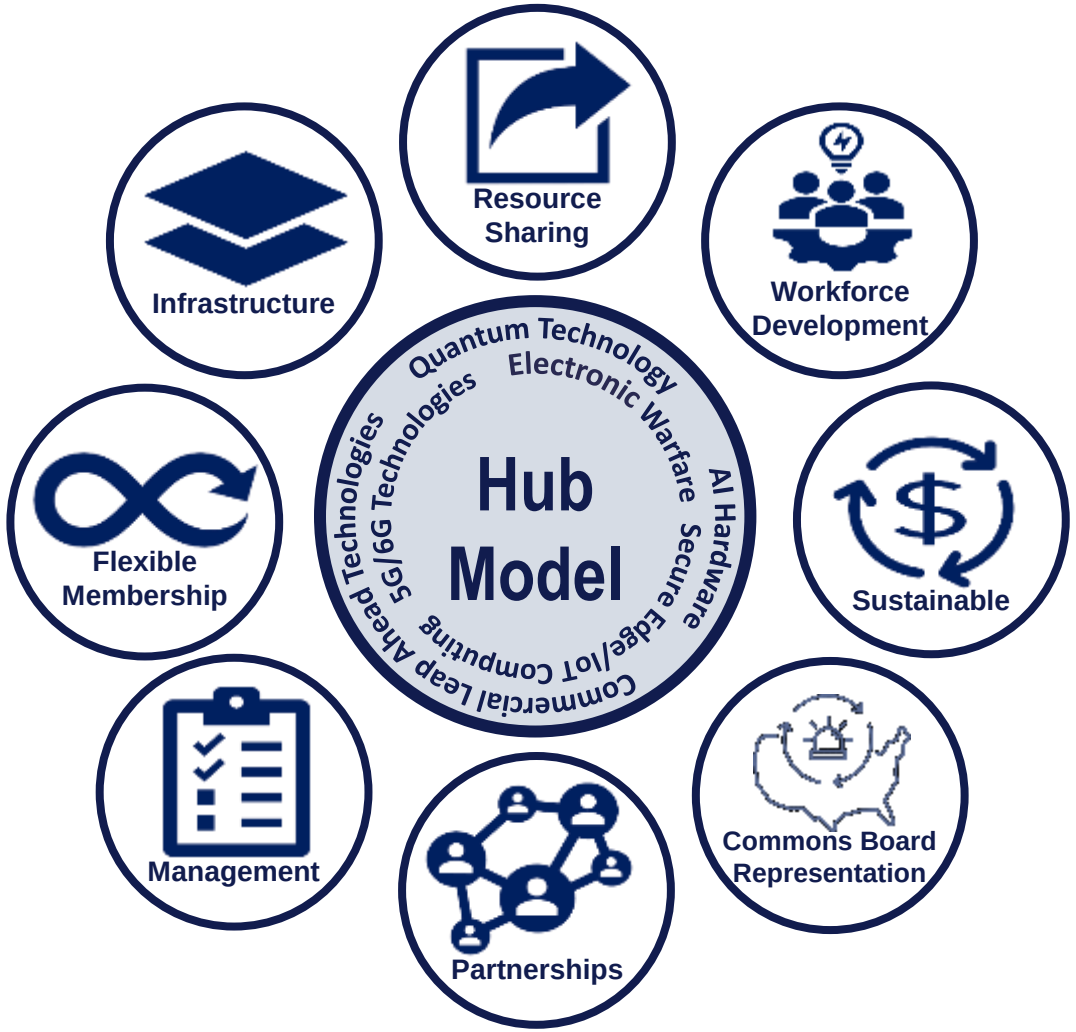

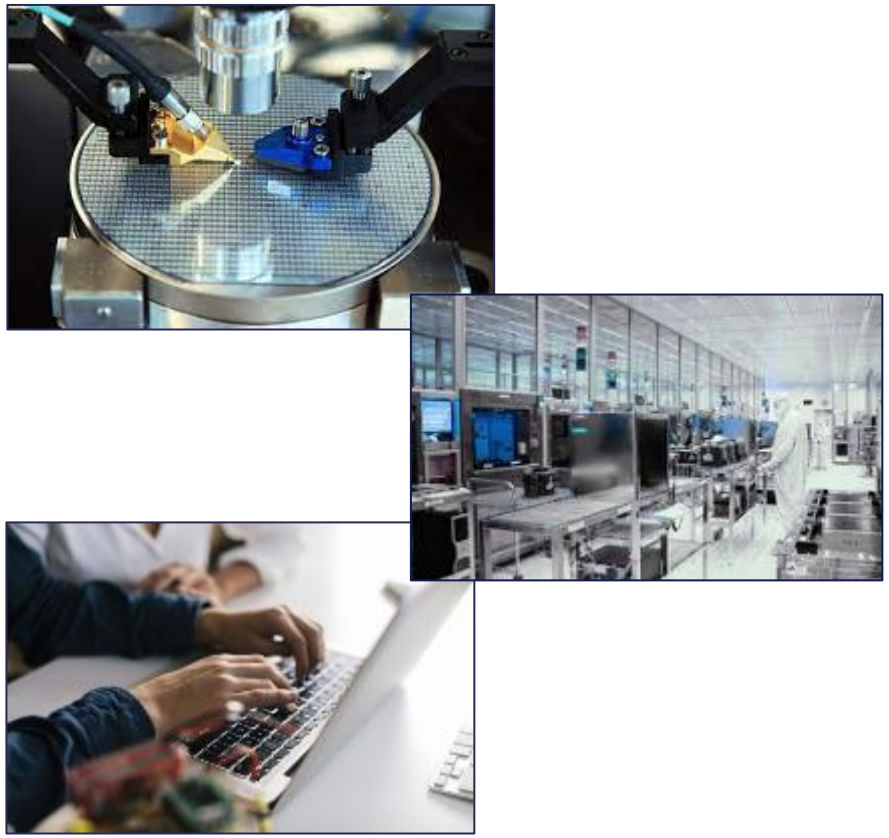

Core Facilities positioned to engage with industry and Government to provide production capacity and commercialization

Hubs have the flexibility to develop a model that ensures participation from all interested stakeholders and sustains the hub in the long term

How to Submit your Questions

The Naval Surface Warfare Center – Crane (NSWC Crane) Strategic & Spectrum Missions Advanced Resilient Trusted Systems (S²MARTS) Other Transaction Authority (OTA) will be the primary contract vehicle for the Microelectronics Commons

The Microelectronics Commons Consortium Manager, the National Security Technology Accelerator (NSTXL), will make program announcements (Events, Documentation changes, etc.) on the S²MARTS site and on www.sam.gov

Important Links

- Microelectronics – DoD Research & Engineering, OUSD(R&E) (cto.mil): *https://www.cto.mil/ct/microelectronics/*
- Microelectronics Commons NSTXL: *https://nstxl.org/opportunity/microelectronics-me-commons/*
  - To submit any questions, locate “Submit a Question” on that site, complete the fields, and click “Submit”.